BIPOLAR JUNCTION TRANSISTORS

- Two junction, three terminal device

- Current directions and voltage

\[ i_c \rightarrow V_{BE} \rightarrow V_{CE} \rightarrow i_e \]

NPN

(a) NPN

(b) PNP
<table>
<thead>
<tr>
<th>Condition</th>
<th>E-B Junction</th>
<th>C-B Junction</th>
<th>Region of Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>Forward biased</td>
<td>Reverse (or un-) biased</td>
<td>Active</td>
</tr>
<tr>
<td>II</td>
<td>Forward biased</td>
<td>Forward biased</td>
<td>Saturation</td>
</tr>
<tr>
<td>III</td>
<td>Reverse biased</td>
<td>Reverse (or un-) biased</td>
<td>Cutoff</td>
</tr>
<tr>
<td>IV</td>
<td>Reverse biased</td>
<td>Forward biased</td>
<td>Inverted</td>
</tr>
</tbody>
</table>

Biasing the NPN transistor for active operation

Switch 1 closed, switch 2 open
Switch 2 closed, switch 1 open

Switch 1 and switch 2 closed; NPN transistor operating in the active region
Operate Regions

Active:

Saturation:

Cutoff:

- Base region lightly doped
- Base region is thin
To have mostly election flow and also have through flow.

(reverse biased or open) $i_B = 0 \Rightarrow i_C = 0$
Transistor Currents

\[ i_E = i_C + i_B \] — (1)
\[ i_C = \alpha i_E \] — (2)
\[ i_C = \beta i_B \] — (3)

Using (1), (2) and (3)

\[ \beta = \frac{\alpha}{1-\alpha} \]

SHOCKLEY

\[ i_E = I_{ES} \left[ \exp \left( \frac{v_{BE}}{V_T} \right) - 1 \right] \] — (4)

Same as diode equation with \( n = 1 \)

Because of (2), we get

\[ i_C = \alpha I_{ES} \left[ \exp \left( \frac{v_{BE}}{V_T} \right) - 1 \right] \] — (5)

From (1) and (2)

\[ i_B = (1-\alpha) i_E \] — (6)

Using (4) and (6), we get

\[ i_B = (1-\alpha) I_{ES} \left[ \exp \left( \frac{v_{BE}}{V_T} \right) - 1 \right] \]
**PNP currents**

Equations 1, 2, and 3
same as for NPN (previous page)

For Shockley equations,
replace $V_{BE}$ with $-V_{BE}$.

For example

$$i_E = I_E \left[ \exp \left( \frac{-V_{BE}}{V_T} \right) - 1 \right]$$
Common Emitter Characteristics

\[ V_{BC} = V_{BE} - V_{CE} \]

For \( V_{BC} \) to be negative (to produce reverse biased EB junction), we need \( V_{CE} > V_{BE} \).

- Fix \( i_B \) by fixing \( V_{BB} \), then vary \( V_{CC} \) to plot \( i_C \) versus \( V_{CE} \) for a constant \( i_B \).

Saturation Region \((V_{CE} < V_{BE})\)

Active Region \((i_C = \beta i_B)\)

\( i_B = 40mA \)

\( V_{CE} (V) \)

Cutoff \((i_B = 0)\)
Input Characteristics

Output Characteristics

Amplification \( i_C = \beta i_B \)

\[ \beta = \frac{5 \text{ mA}}{50 \mu \text{A}} = 100 \]

\[ \beta_{ac} = \frac{\Delta i_C}{\Delta i_B} = \frac{1 \text{ mA}}{10 \mu \text{A}} = 100 \]
Load-line Analysis of a Common-Collector Amplifier

Using KVL in the left loop, we get

\[ V_{BB} + V_{in}(t) = R_b i_B(t) + v_{BE}(t) \]  \( -1 \)

Output circuit

\[ V_{CC} = i_C R_C + V_{CE} \]
**EXAMPLE:**

\[ V_{in}(t) = 0.4 \sin(2000\pi t) \]

**INPUT EQUATION**

For \( V_{in} = 0 \)

\[ V_{bb} + V_{in} = R_E i_B + V_{BE} \]

\[ 1.6 + 0.4 = 40,000 i_B + V_{BE} \]

When \( i_B = 0 \) \( \Rightarrow V_{BE} = 1.6 \) V

When \( V_{BE} = 0 \) \( \Rightarrow i_B = 40 \mu A \)

For Point 1, \( i_B = 25 \mu A \)

For Point 2, \( i_B = 35 \mu A \)

For Point 3, \( i_B = 5 \mu A \)

**OUTPUT EQUATION**

\[ V_{CC} = R_C i_C + V_{CE} \]

When \( i_C = 0 \) \( \Rightarrow V_{CE} = V_{CC} = 10 \) V

When \( V_{CE} = 0 \) \( \Rightarrow i_C = \frac{V_{CE}}{R_C} = \frac{10}{2000} \) Amps = 5 mA

**Graphical Analysis:**

- Peak to peak input voltage = 0.8 V
- Peak output = 4 V

\[ \text{Voltage gain} = \frac{4}{0.8} = 5 \]

\[ \therefore -5 \text{ V out sign showing signal inversion} \]
Figure 5.9 Load-line analysis for Example 5.2.
Figure 5.10  Voltage waveforms for the amplifier of Figure 5.7. See Example 5.2.
DISTORTION

- The output is not a TRUE sinusoid depending on the input/output characteristics of the amplifier (transistor).

Secondary Effects:

Ideal model: First order model
Real BJTs show secondary effects.

Collector Breakdown effect

Also: βac changing due to non-uniform spacing

\[ V_{CE}(V) \quad (\beta_{ac} = \frac{\Delta i_c}{\Delta i_b}) \]
- $\beta$ also varies from unit to unit.
- Typically ratio of highest value to lowest value of $\beta = 3:1$
- $\beta$ also varies with temperature
- $\beta$ and $\beta_{ac}$ also vary with $V_c$

Since $\beta$ and $\beta_{ac}$ vary, therefore many times $\beta$ and $\beta_{ac}$ used interchangeably; and also create designs which are insensitive to $\beta$ variations.

- **Input characteristics, secondary effect**

- Input curves change with $V_{CB}$.
- IF $V_{CE} > 0.2V$ (here) then practically same curve.

- **High Frequency (Charge Storage Effects)**

  At high frequency we add capacitors in the BJT model (e.g. between $B$ and $C$, and $B$ and $E$ etc.)
Common-emitter amplifier using PNP
Common-emitter characteristics for a pnp BJT.
Figure 5.20

BJT large-signal models. (Note: Values shown are appropriate for typical small-signal silicon devices at a temperature of 300 K.)
(a) Output characteristic

Saturation region
\[ I_C < \beta I_B \]
Active region
\[ I_C = \beta I_B \]
Cutoff region
\[ I_B = I_C = 0 \]

(b) Input characteristic

Active or saturation regions

Cutoff
Large Signal DC Analysis.

Just like diode analysis assume a region of operation and then check for consistency.

**EXAMPLE**

\[
\begin{align*}
V_C & = 15V \\
V_B & = 15V \\
\beta & = 100
\end{align*}
\]

Assume: \( V_{BE} = \text{cut-off} \)

\[
\begin{align*}
V_{BE} & = 0.7V \\
V_{CE} & = 0.2V \\
I_B & = \frac{15 - 0.7}{200k\Omega} = 71.5mA \\
I_C & = \frac{15 - 0.2}{1k\Omega} = 14.8mA
\end{align*}
\]

Here \( V_{BE} = 15 \) \( (\text{for cut-off} \) \( V_{BE} < 0.5 \) \) \( \text{inconsistency} \)

Saturation:

\[
\begin{align*}
V_C & = 15V \\
V_B & = 15V \\
\beta & = 100 \\
I_B & = \frac{15 - 0.7}{200k\Omega} = 71.5mA \\
I_C & = \beta I_B = 715mA
\end{align*}
\]

Here \( \beta I_C < I_C \) \( (\text{should be } > \text{ for saturation}) \)

Inconsistent also

Active:

\[
\begin{align*}
V_C & = 15V \\
V_B & = 15V \\
\beta & = 100 \\
I_B & = \frac{15 - 0.7}{200k\Omega} = 71.5mA \\
I_C & = \beta I_B = 71.5mA
\end{align*}
\]

\[ V_{CE} = 15 - I_C(1k\Omega) = 7.85V \]

\[ \therefore V_{CE} > 0.2V \text{ and } I_B > 0 \]

Transistor operates in **Active region**.
BASE BIAS

- $I_B$ is controlled by $V_{cc}$ and $R_B$
- A point sensitive to change in $\beta$

EXAMPLE 5.4 + 55

$\alpha$ point for $\beta = 100$

$\alpha$ point for $\beta = 300$

A 1:3 variation is expected.
- Using this circuit, $R_B$ would have to be adjusted
to get $\alpha$ in the middle (not practical)
- We need $\alpha$ in the middle so that the AC
  signal can be amplified without distortion
  (class A amplifiers)

$IC$ (point at middle)

$\alpha$ close to cut off

..also causes thermal runaway... because higher beta causes
higher IC causing higher beta...
Assuming active region, we get (B) from (A)

\[ V_{BB} = 0.7 + I_E R_E \]

\[ \therefore I_E = \frac{V_{BB} - 0.7}{R_E} \quad (\text{Independent of } \beta) \]

\[ I_C = \beta I_B \quad \text{and} \quad I_E = I_B + I_C \]

\[ \therefore I_E = (\beta + 1) I_B \]

\[ \therefore I_B = \frac{I_E}{\beta + 1} \]

\[ \therefore I_C = \frac{\beta I_B}{1 + \beta} \quad (\text{Fairly constant for high } \beta) \]

\[ V_{cc} = R_C I_C + V_C E + R_E I_E \]

\[ V_C E = V_{cc} - R_C I_C - R_E I_E \quad (\text{Fairly constant again because of } I_C) \]

**NOT VERY PRACTICAL STILL**

- Two sources required (\( V_{BB} \) and \( V_{cc} \))
- For AC signals, the base is at ground (\( \therefore \) doesn't allow AC signals to be fed at base).
**Voltage Divider Bias**

\[ V_B = \frac{R_2 V_{cc}}{R_1 + R_2} \]

\[ R_B = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}} \]

Usually \( V_{BE} = 0.7 \) V

\[ V_B = R_B I_B + V_{BE} + R_E I_E \quad (1) \]

\[ \therefore I_E = (\beta + 1) I_B \quad (2) \]

From (1) and (2)

\[ I_B = \frac{V_B - V_{BE}}{R_B + (\beta + 1) R_E} \quad (3) \]

\[ V_{CE} = V_{cc} - R_C I_C - R_E I_E \quad (4) \]

where \( I_C = \beta I_B \) and \( I_E = (\beta + 1) I_B \quad (5) \)

Use (3) in (4) using (5) to solve for \( V_{CE} \).
DESIGN CONSIDERATIONS FOR VOLTAGE DIVIDER BIAS

Recall \[ I_B = \frac{V_B - V_{BE}}{R_B + (\beta + 1)R_E} \]
and \[ I_C = \beta I_B \quad \text{and} \quad I_E = (\beta + 1)I_B \]

\[ \therefore \text{If } \beta \text{ is large and } R_B \text{ is small, then} \]
\[ I_C = \beta I_B = \frac{\beta (V_B - V_{BE})}{R_B + (\beta + 1)R_E} \]
\[ = \frac{V_B - V_{BE}}{R_E} \quad \text{(independent of } \beta) \]

Same for \( I_E \)...

\[ \therefore V_{CE} = V_{CC} - R_CI_C - R_EL_E \quad \text{(sensitive to } \beta \text{ variation)} \]

If \( R_E \) large, then \( I_C \) and \( V_{CE} \) vary with \( \beta \).
So, keep \( R_1 \) and \( R_2 \) small.

However, both \( R_1 \) and \( R_2 \) \( \rightarrow \) larger currents,
overheating & need for larger (expensive) power supply.

\[ \therefore \text{Compromise values of } R_1 \text{ and } R_2 \]

- Choose \( R_2 \) so that current through \( R_2 = 10 \) (or 20 times) largest \( I_B \) expected.

- \[ I_B = \frac{V_B - V_{BE}}{R_B + (\beta + 1)R_E} \quad \text{and } V_{BE} \text{ varies with temperature,} \]
make \( V_B \) larger than variations

- \[ V_B = \frac{1}{3} V_{CC} \quad \text{V(ce over } R_E) = \frac{1}{3} V_{CC} = V(ce over } R_E) = V_C \]

- Use frequency response, peak signal swing, availability, cost etc. Constraints also.
TRANSISTOR MAXIMUM RATINGS

Maximum ratings on

\[ V_{EB}, V_{CB}, V_{CE} \] voltages

\[ I_{C}(\text{max}), P_{D}(\text{max}) \] (power)

\[ T_{j}(\text{max}) \] junction temperature

\[ P_{D}(\text{max}) \text{ curve} \leq V_{CE} I_{C} \]

\[ T_{j} = T_{a} + \Theta_{JA} P_{D} \]

\[ \uparrow \] power dissipation

\[ \downarrow \text{junction temperature} \]
\[ \uparrow \text{ambient temperature} \]

'\text{as this } \beta \text{ decreases with } \text{temperature}.'
\[ i_B(t) = I_{BA} + i_b(t) \]
\[ v_{BE}(t) = V_{BEA} + v_{BE}(t) \]
\[ i_D = (1 - \alpha) I_{ES} \left[ \exp \left( \frac{v_{BE}}{V_T} \right) - 1 \right] \]
\[ I_{BA} + i_b(t) = (1 - \alpha) I_{ES} \exp \left( \frac{V_{BEA} + v_{BE}(t)}{V_T} \right) \]
\[ = (1 - \alpha) I_{ES} \exp \left( \frac{V_{BEA}}{V_T} \right) \exp \left( \frac{v_{BE}(t)}{V_T} \right) \]

\[ \therefore I_{BA} + i_b(t) = I_{BA} \exp \left( \frac{v_{BE}(t)}{V_T} \right) \]

Here, \( v_{BE} \) is very small, so using \( \exp(1) \approx 1 + 1 \frac{v_{BE}}{V_T} \) for \( |x| \ll 1 \).

\[ I_{BA} + i_b(t) \approx I_{BA} \left( 1 + \frac{v_{BE}(t)}{V_T} \right) \]

\[ i_b(t) = \frac{I_{BA} v_{BE}(t)}{V_T} \]

\[ \text{define } \frac{V_T}{I_{BA}} = \frac{\eta}{I_{ES}} \]

\[ \text{then } \frac{i_b(t)}{V_{BE}} = \frac{v_{BE}(t)}{V_T} \]

\[ \text{since } I_{BA} = I_{ES} / \beta \Rightarrow \eta = \frac{\beta V_T}{I_{ES}} \]

\[ \text{Typical value of } \eta = 2600 \]

\[ \text{Total current } i_C(t) = \beta i_b(t) \]

\[ \text{also } I_{CA} = \beta I_{BA} \]

\[ I_{CA} + i_C(t) = \beta I_{BA} + \beta i_b(t) \]

\[ \therefore i_C(t) = \beta i_b(t) \]
Small Signal Model for BJT

- Small signal model is EXACTLY the same for NPN and PNP.

![Circuit Diagram]

- Coupling Capacitors:
  - Input coupling capacitor
  - Output coupling capacitor

For DC, capacitor is open, so DC circuit is → which gives us a point.

For AC, capacitor is a short.

Capacitor Impedance = \( \frac{1}{j \omega C} \) (\( \omega \) at high frequency but large (\( \infty \)).

- If the signal has very low frequency then capacitor is not a short, and at very high frequency, the model for BJT is changed (additional capacitances added).

For low impedance to AC

- This analysis true for mid frequency range

  \[
  X_C \approx R_C + \frac{R_L + Z_0}{10}
  \]

  \[
  X_C \leq \frac{R_L + Z_0}{10}
  \]
(a) Actual circuit

(b) Small-signal ac equivalent circuit

(c) Equivalent circuit used to find $Z_o$

Figure 5.32 Common-emitter amplifier.
Common Emitter Amplifiers (Small Signals)

**VOLTAGE GAIN**

\[ V_{in} = V_{be} = i_b R_i \]
\[ V_o = -R_C \beta i_b \]
\[ A_v = \frac{V_o}{V_{in}} = -\frac{R_C}{R_i} \]

-ve sign to show inverting amplifier.

Also \( A_v^o = -\frac{\beta R_C}{R_i} \)

**LARGE VOLTAGE GAIN** for Common Emitter.

**INPUT IMPEDANCE**

\[ R_i = \frac{V_{in}}{I_{in}} = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_i}} \]

**CURRENT GAIN**

\[ A_i = \frac{I_o}{I_{in}} = \frac{A_v}{R_C} \]

**POWER GAIN**

\[ G = A_i A_v \]

**OUTPUT IMPEDANCE**

Let source voltage = 0 and then look at impedance from the output terminals.

\[ Z_o = R_C \]
(a) Actual circuit

(b) Small-signal equivalent circuit

(c) Equivalent circuit used to find output impedance $Z_o$

**Figure 5.35** Emitter follower.
EMITTER FOLLOWER (Small Signal)

**VOLTAGE GAIN**

\[ V_o = R'_e (1+\beta) i_b \quad - (1) \]

\[ V_i = h_{fe} i_b + (1+\beta) i_b R'_e \quad - (2) \]

\[ A_v = \frac{R'_e (1+\beta)}{h_{fe} + (1+\beta) R'_e} \quad - (3) \]

*(notice \( A_v < 1 \) (close to 1)*

*non-inverting follower*

*can provide current gain*

**INPUT IMPEDANCE**

\[ Z_i = \frac{1}{h_{fe} + R'_e + \frac{1}{Z_{ic}}} \quad - (4) \]

\[ Z_{ic} = \frac{V_i}{V_o} \quad (use \ (2)) \]

\[ \frac{V_o}{V_i} \]

*relatively high compared to other BJT configurations*

*can get higher using FETs, and also using feedback*

**OUTPUT IMPEDANCE**

*Remove load*

*Current signal sources*

*Load in from output terminals*

\[ Z_o = \frac{V_o}{i_b} \quad - (5) \]

\[ KCL \ at \ output \ node \Rightarrow \]

\[ i_b + \beta i_b + i_x = \frac{V_o}{R_e} \quad - (6) \]

**define**

\[ R'_s = \frac{1}{h_{fe} + \frac{1}{R'_s} + R'_2} \quad - (4) \]

\[ KVL \ at \ output \ outside \ loop \ all \ the \ way \]

\[ V_o + \beta i_b + R'_s i_b = 0 \quad - (8) \]

*replace \( i_b \) in \( (6) \) using \( (8) \) to get*

\[ Z_o = \frac{1}{\frac{V_o}{i_b}} = \frac{1}{\frac{V_o}{i_b}} \quad - (7) \]

\[ \frac{(1+\beta)}{(R'_e + R'_2)} R_e \]

*Which is \( Z_o = R_e \| Z_{tot} \)*

*where \( Z_{tot} = \frac{R'_s + h_{fe}}{1+\beta} \)*

*relatively low output impedance*
Common-base amplifier circuit.
\[ V_{in} = -r_{\pi} I_b \]

\[ V_o = -\beta I_b R'_L \]

\[ A_v = \frac{V_o}{V_{in}} = \frac{\beta R'_L}{r_{\pi}} \]

\[ L_{in} = \frac{V_{in}}{R_E} - (\beta+1) I_b \]

\[ L_{in} = \frac{V_{in}}{R_E} + \frac{\beta+1}{r_{\pi}} V_{in} \]

\[ R_{in} = \frac{V_{in}}{I_m} = \frac{1}{R_E} + \frac{\beta+1}{r_{\pi}} \]

*Output resistance:*

\[ \frac{V_i}{R_S} + \frac{V_i}{R_E} = I_b + \beta I_b \]

\[ V_i = -r_{\pi} I_b \]

\[ \begin{align*}
L_b + \beta I_b + \frac{r_{\pi}}{R_S} I_b + \frac{r_{\pi}}{R_E} I_b &= 0 \\
\therefore I_b &= 0 \\
R_o &= \frac{V_x}{I_x} = R_c
\end{align*} \]
SUMMARY (Section 5.12)

- Drawing small signal equivalent circuit
  1. Replace ac voltage supply by a short.
  2. " " current " " open circuit.
  3. For mid frequency analysis, replace capacitors by shorts.
  4. Replace inductors by open circuit.
  5. Replace transistor with its equivalent circuit.

- Identify circuit variables of interest

- Finding output impedance
  1. Turn off independent sources (voltage & current; make them zero)
  2. Remove the load
  3. Find impedance looking in from output terminals
    (might have to feed in test voltage Vx and then divide that by Ix)

- Write circuit equations
- Find and check the desired expression
- Check units
(a) Common-emitter amplifier with unbypassed emitter resistor

(b) Variation of the emitter follower using a dc current source for biasing

(c) Variation of the common-base amplifier [assume that the radio-frequency choke (RFC) is an open circuit for the ac signals]

Figure 5.40 Amplifier circuits.
Figure 5.41  Small-signal equivalent circuits for the circuits of Figure 5.40.
Summary of Amplifier Configurations

<table>
<thead>
<tr>
<th></th>
<th>Common Base</th>
<th>Common Collector</th>
<th>Common Emitter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic circuit</td>
<td>![Common Base Diagram]</td>
<td>![Common Collector Diagram]</td>
<td>![Common Emitter Diagram]</td>
</tr>
<tr>
<td>Power gain</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes (highest)</td>
</tr>
<tr>
<td>Voltage gain</td>
<td>Yes</td>
<td>No (less than 1)</td>
<td>Yes</td>
</tr>
<tr>
<td>Current gain</td>
<td>No (less than 1)</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Input impedance</td>
<td>Lowest (≈50 Ω)</td>
<td>Highest (≈300 kΩ)</td>
<td>Medium (≈1 kΩ)</td>
</tr>
<tr>
<td>Output impedance</td>
<td>Highest (≈1 MΩ)</td>
<td>Lowest (≈300 Ω)</td>
<td>Medium (≈50 kΩ)</td>
</tr>
<tr>
<td>Phase inversion</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Application</td>
<td>Used mainly as an RF amplifier</td>
<td>Used mainly as an isolation amplifier</td>
<td>Universal—works best in most applications</td>
</tr>
</tbody>
</table>
High-impedance signal source

Common-collector stage (provides isolation)

Common-emitter stage

Output signal
BJT as a SWITCH (or an Inverter)

\[ V_{out} = V_{cc} \quad (0.3 \text{V saturation}) \]

\[ V_{out} = (V_{in})^c \quad (V_{out} = \text{complement of } V_{in}) \]

**Condition in cutoff**
\[ V_{ce} = V_{cc} \]

**Condition in Saturation**
\[ I_C = \frac{V_{cc} - 0.2}{R_C} \quad (\text{saturation}) \]

Minimum Value of \( I_B \) needed for saturation:
\[ I_C(\text{sat}) \]

Equation to calculate \( I_B \) (using input characteristic)

\[ V_{BB} = I_B R_B + 0.7 \]
**RTL logic (Inverter)**

\[ V_o = V_{cc} - R_c I_c \]

\[ I_c = \beta I_B \quad \Rightarrow \quad I_B = \frac{V_{in} - 0.7}{R_B} \]

\[ V_o = V_{cc} - R_c \frac{V_{in} - 0.7}{R_B} \]

\[ V_o < 0.2 \text{, then } V_o = 0.2 \quad (\text{saturation}) \]

\[ V_{in} < 0.7 \text{ then } V_o = V_{cc} \quad (\text{cut-off}) \]

**NOR logic**

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>( V_{out} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

\( S = \overline{A} \text{ and } \overline{A} \text{ opposite logic} \)

\[ S \Rightarrow \overline{Q} = 1, \overline{R} = Q = 0 \]

\( (S, R) = (0, 0) \text{ keep previous state} \)

\( (S, R) = (1, 1) \text{ NOT accepted} \)
Figure 5.47  RS flip-flop.