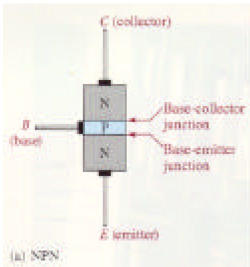
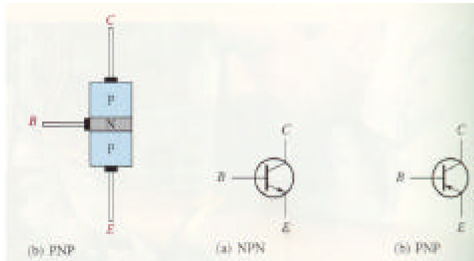
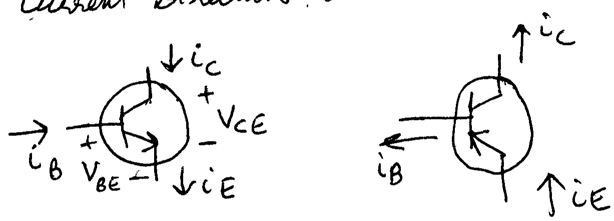
BIPOLAR JUNCTION TRANSISTORS

- Two junction, three terminal device

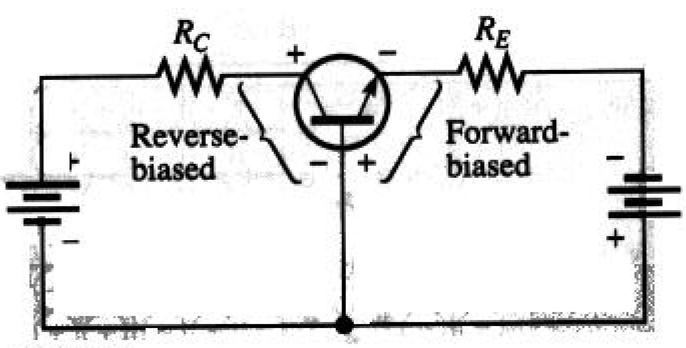




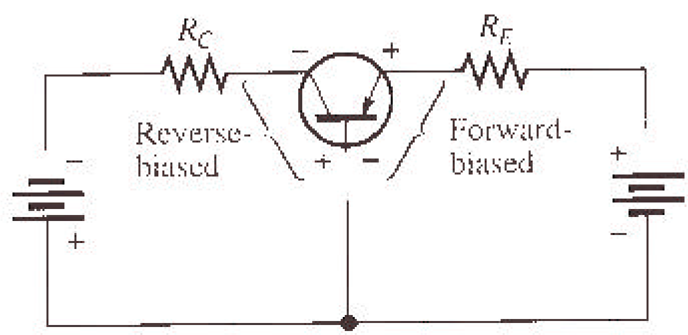
- Current Directions and Voltages



NPN

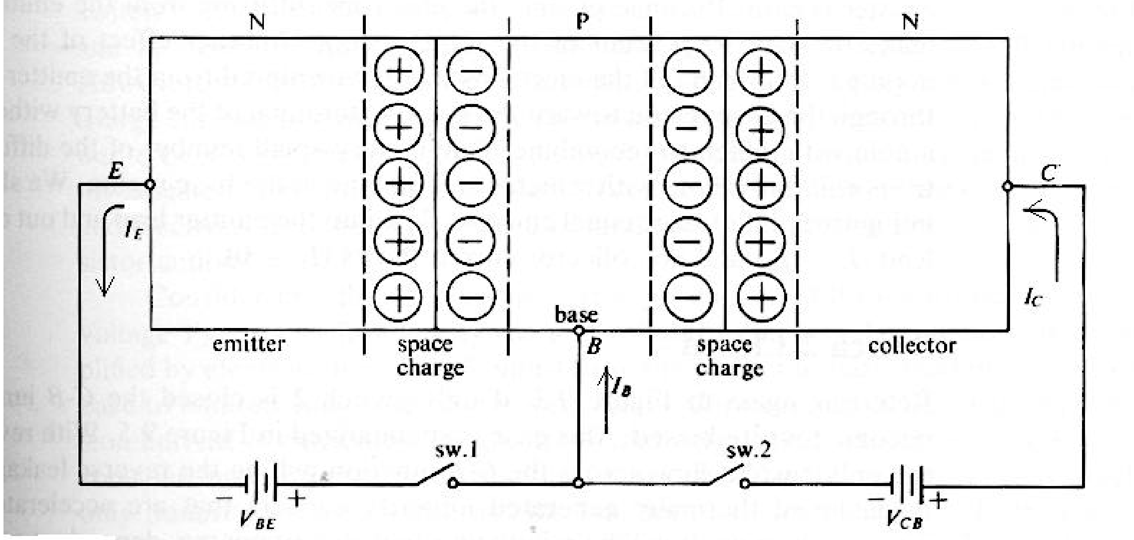


(a) NPN

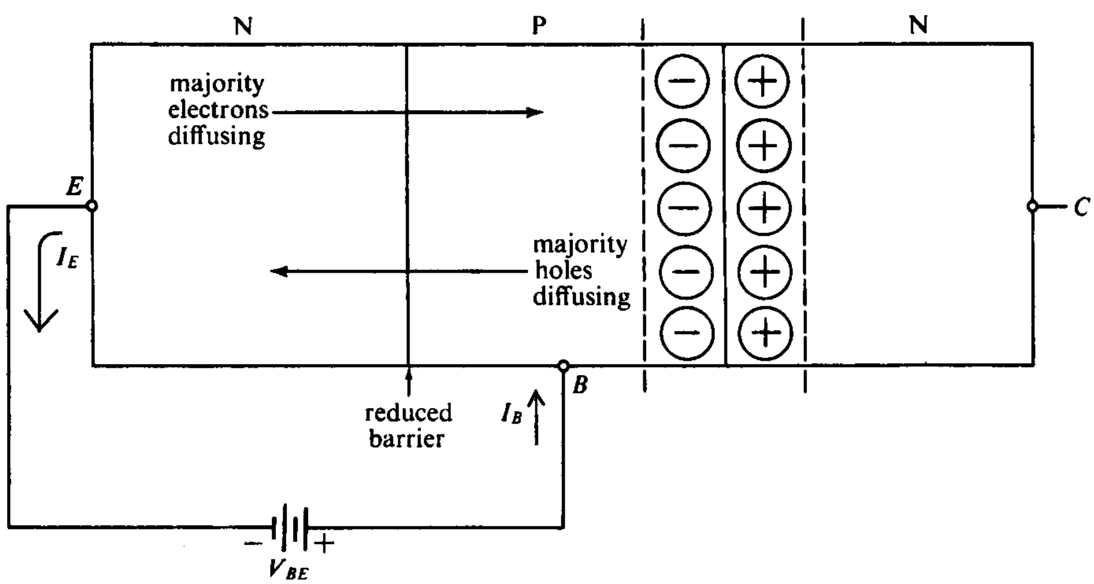


(b) PNP

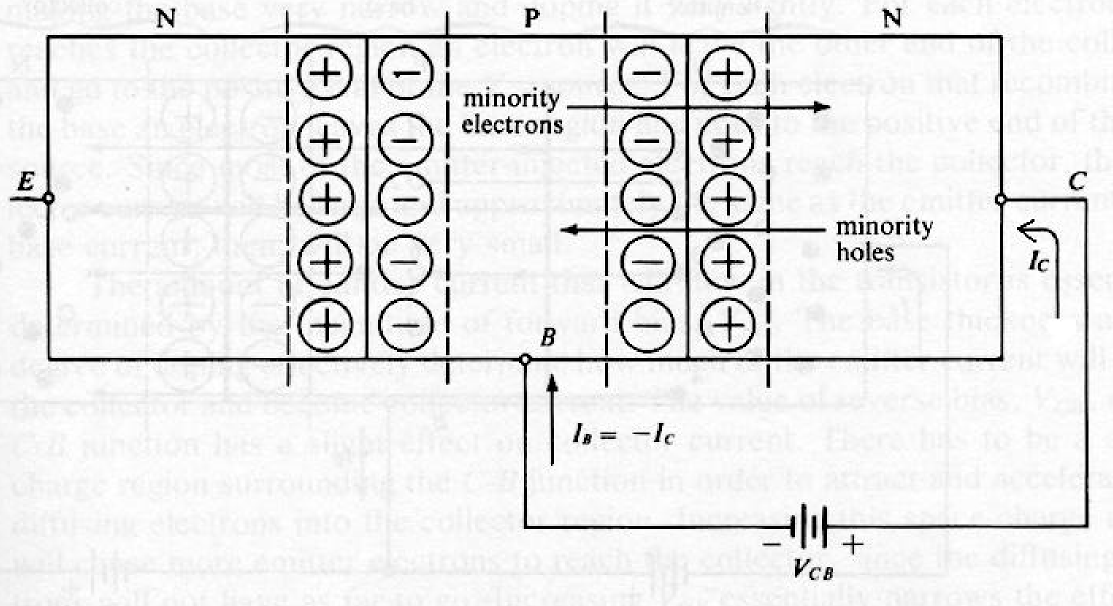
Condition	*E-B Junction*	*C-B Junction*	*Region of Operation*
I	Forward biased	Reverse (or un-) biased	Active
II	Forward biased	Forward biased	Saturation
III	Reverse biased	Reverse (or un-) biased	Cutoff
IV	Reverse biased	Forward biased	Inverted



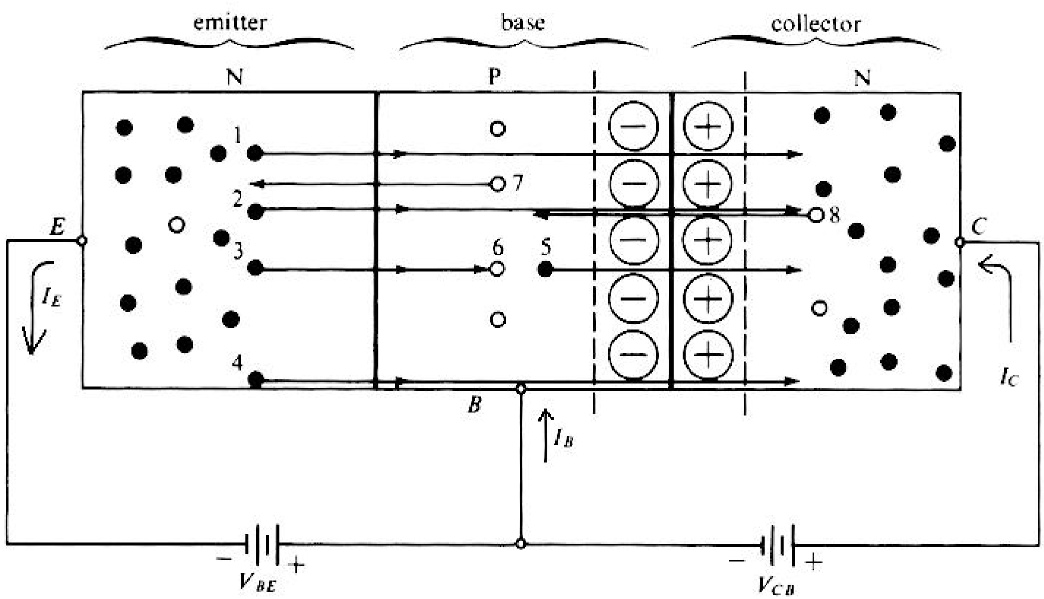
Biasing the NPN transistor for active operation



Switch 1 closed, switch 2 open



Switch 2 closed, switch 1 open



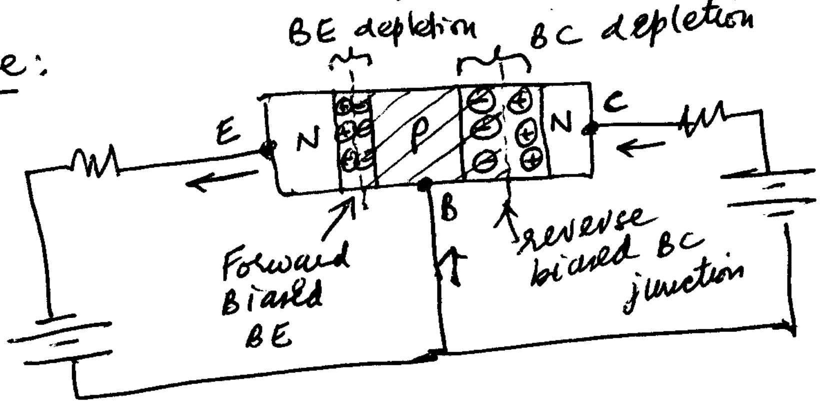
Switch 1 and switch 2 closed; NPN transistor operating in the active region

Operating Regions

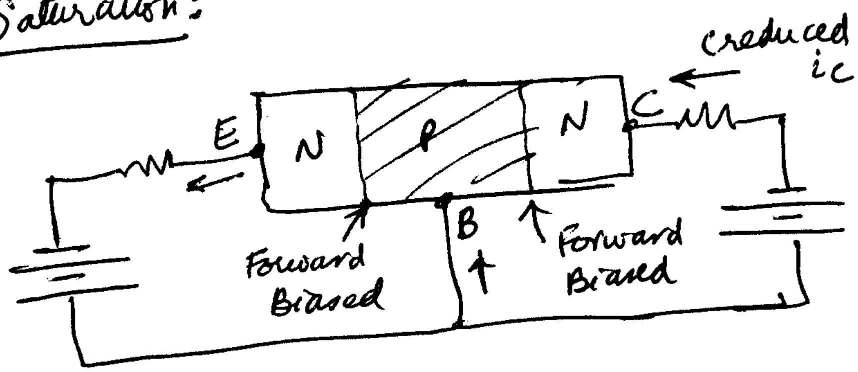
- Base region lightly doped
- Base region is thin

To have mostly electron flow and also have through flow.

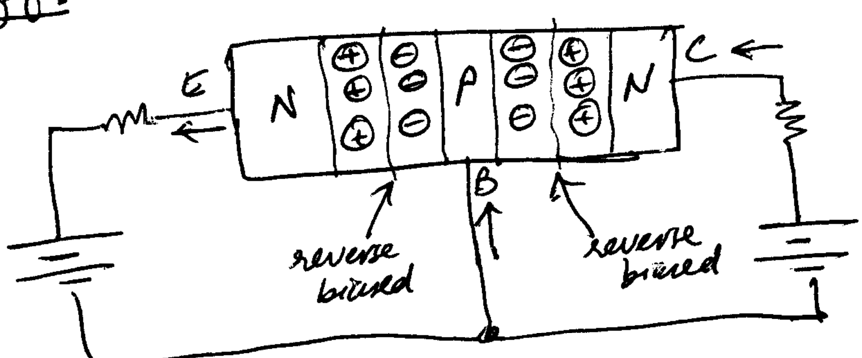
Active:



Saturation:



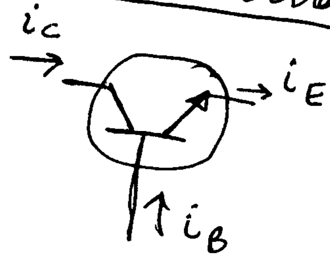
Cutoff:



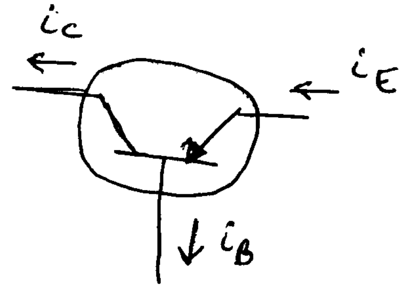
(reverse biased or open)

$i_B = 0 \Rightarrow i_C = 0$

<u>Transistor Currents.</u>



NPN



PNP

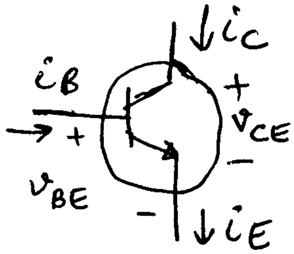
$$\boxed{i_E = i_C + i_B} \quad -\ (1)$$

$$\boxed{i_C = \alpha i_E} \quad -\ (2)$$

$$\boxed{i_C = \beta i_B} \quad -\ (3)$$

Using (1), (2) and (3)

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$



SHOCKLEY

$$\boxed{i_E = I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right]} \quad -\ (4)$$

Same as diode equation with $n = 1$

Because of (2), we get

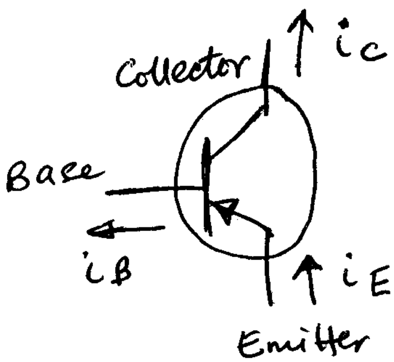
$$\boxed{i_C = \alpha I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right]} \quad -\ (5)$$

From (1) & (2) $\quad i_B = (1-\alpha)\, i_E \quad -\ (6)$

Using (4) in (6), we get

$$\boxed{i_B = (1-\alpha)\, I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right]}$$

PNP currents



PNP

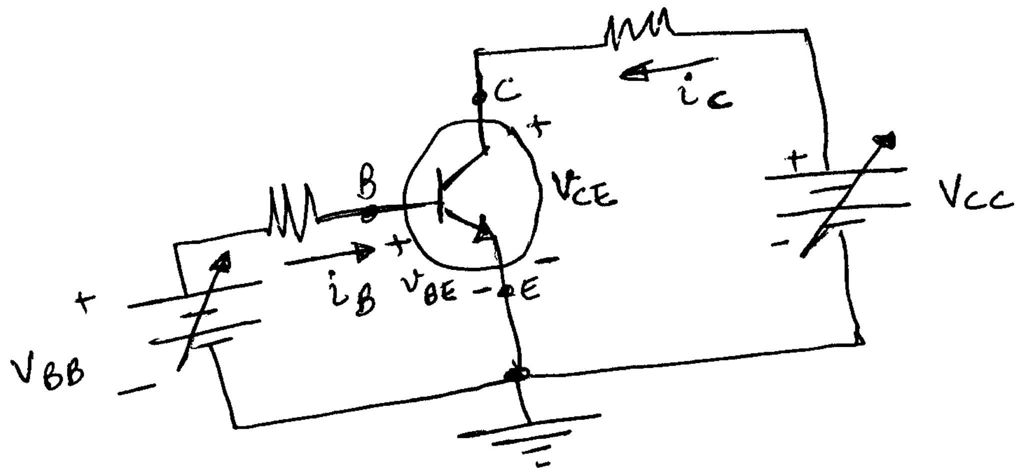
Equations ① , ② and ③ same as for NPN (previous page)

For Shockley equations, replace v_{BE} with $-v_{BE}$.

For example

$$i_E = I_{ES}\left[\exp\left(\frac{-v_{BE}}{V_T}\right) - 1\right]$$

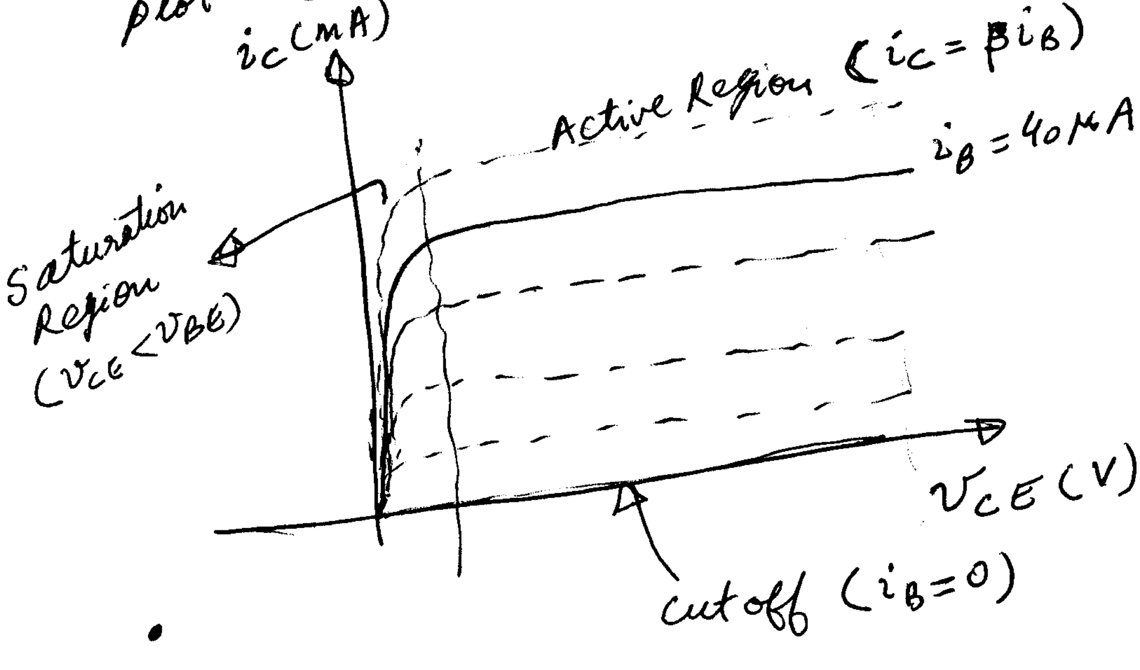
Common Emitter Characteristics



$$v_{BC} = v_{BE} - v_{CE}$$

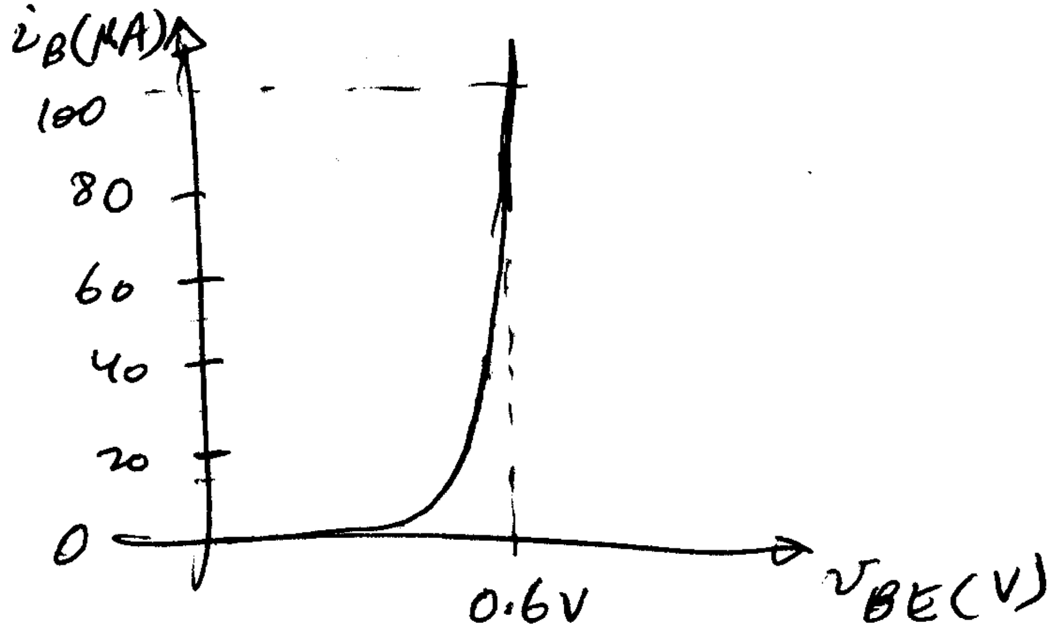
For v_{BC} to be negative (to produce reverse biased EB junction), we need $v_{CE} > v_{BE}$.

- Fix i_B by fixing V_{BB}, then vary V_{CC} to plot i_C versus v_{CE} for a constant i_B.

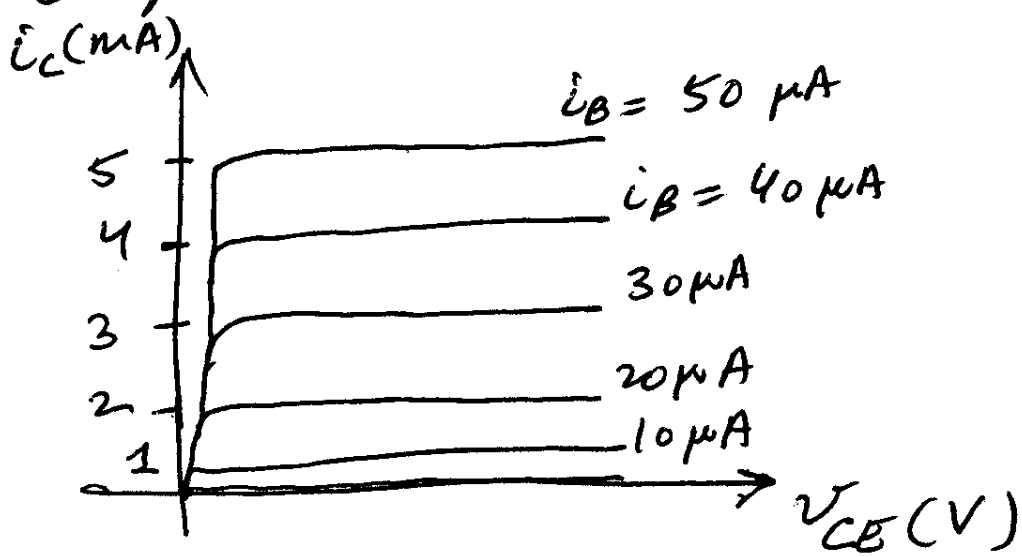


-

Input Characteristics



Output Characteristics

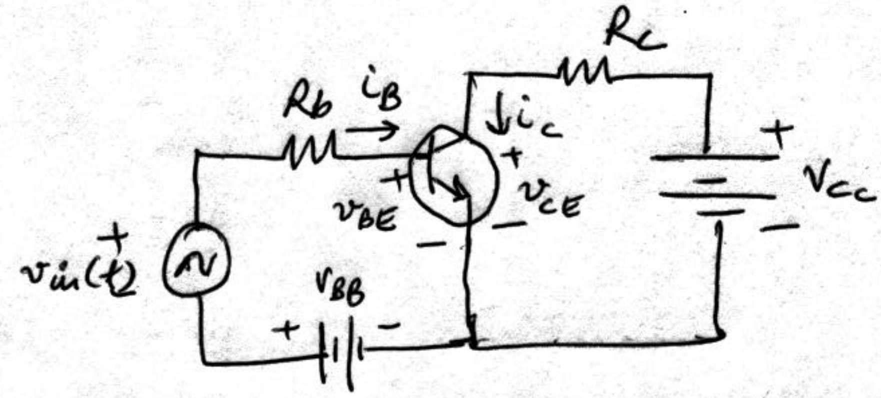


Amplification $i_C = \beta i_B$

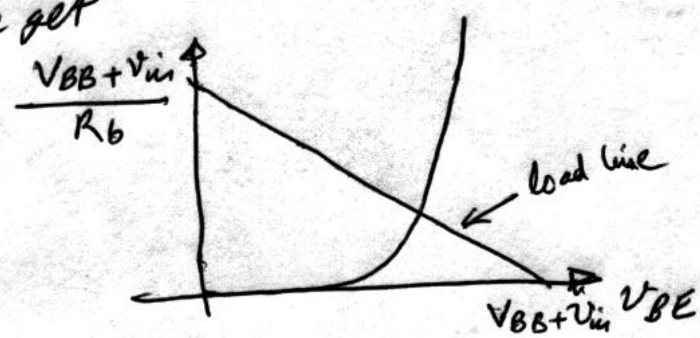
$$\beta = \frac{5\,mA}{50\,\mu A} = 100$$

$$\beta_{ac} = \frac{\Delta i_C}{\Delta i_B} = \frac{1\,mA}{10\,\mu A} = 100$$

Load-line Analysis of a Common-Emitter Amplifier

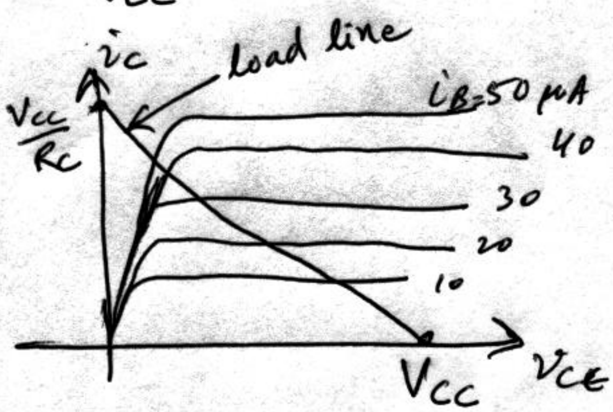


using KVL in left loop, we get $V_{BB} + v_{in}(t) = R_b i_B(t) + v_{BE}(t)$ — (1)

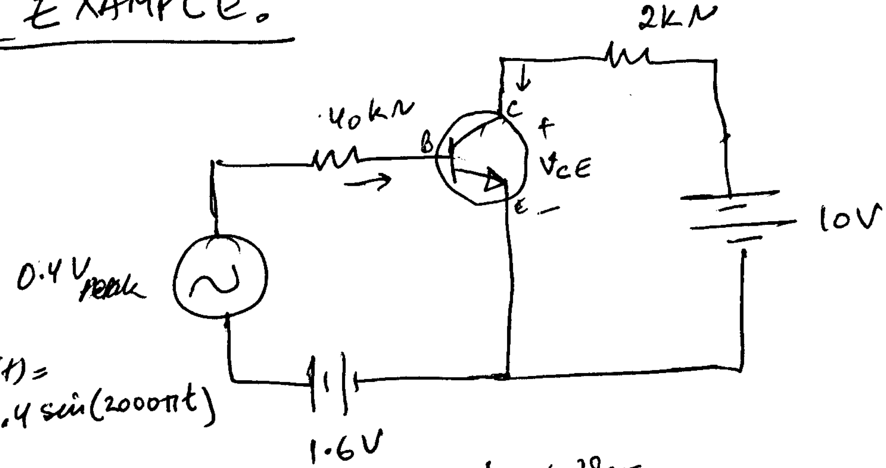


Output circuit

$$V_{CC} = i_C R_C + v_{CE}$$



EXAMPLE:



$v_{in}(t) = 0.4\sin(2000\pi t)$

INPUT EQUATION $V_{BB} + v_{in} = R_B i_B + v_{BE}$

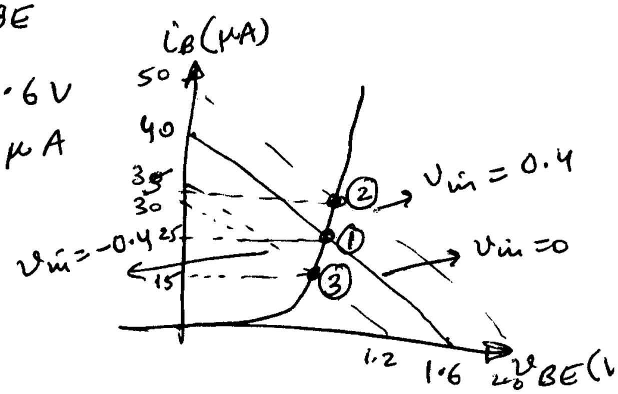
For $v_{in} = 0$: $1.6 + \cancel{v_{in}}^{0} = 40{,}000 i_B + v_{BE}$

when $i_B = 0 \Rightarrow v_{BE} = 1.6V$

" $v_{BE} = 0 \Rightarrow i_B = 40\mu A$

For Point ①, $i_B = 25\mu A$, ② $i_B = 35\mu A$

③, $i_B = 15\mu A$

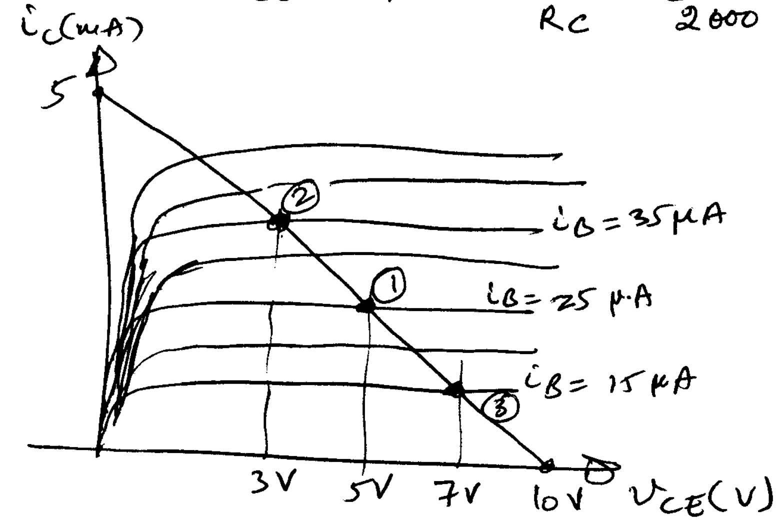


OUTPUT EQUATION

$V_{CC} = R_C i_C + v_{CE}$

when $i_C = 0 \Rightarrow v_{CE} = V_{CC} = 10$

" $v_{CE} = 0 \Rightarrow i_C = \frac{V_{CC}}{R_C} = \frac{10}{2000}$ Amps $= 5mA$.



Peak to Peak input voltage = 0.8V

" " " output " = 4V

$\therefore$ $\boxed{\text{Voltage gain} = \frac{4}{0.8} = 5}$ $= -5$ −ve sign showing signal inversion

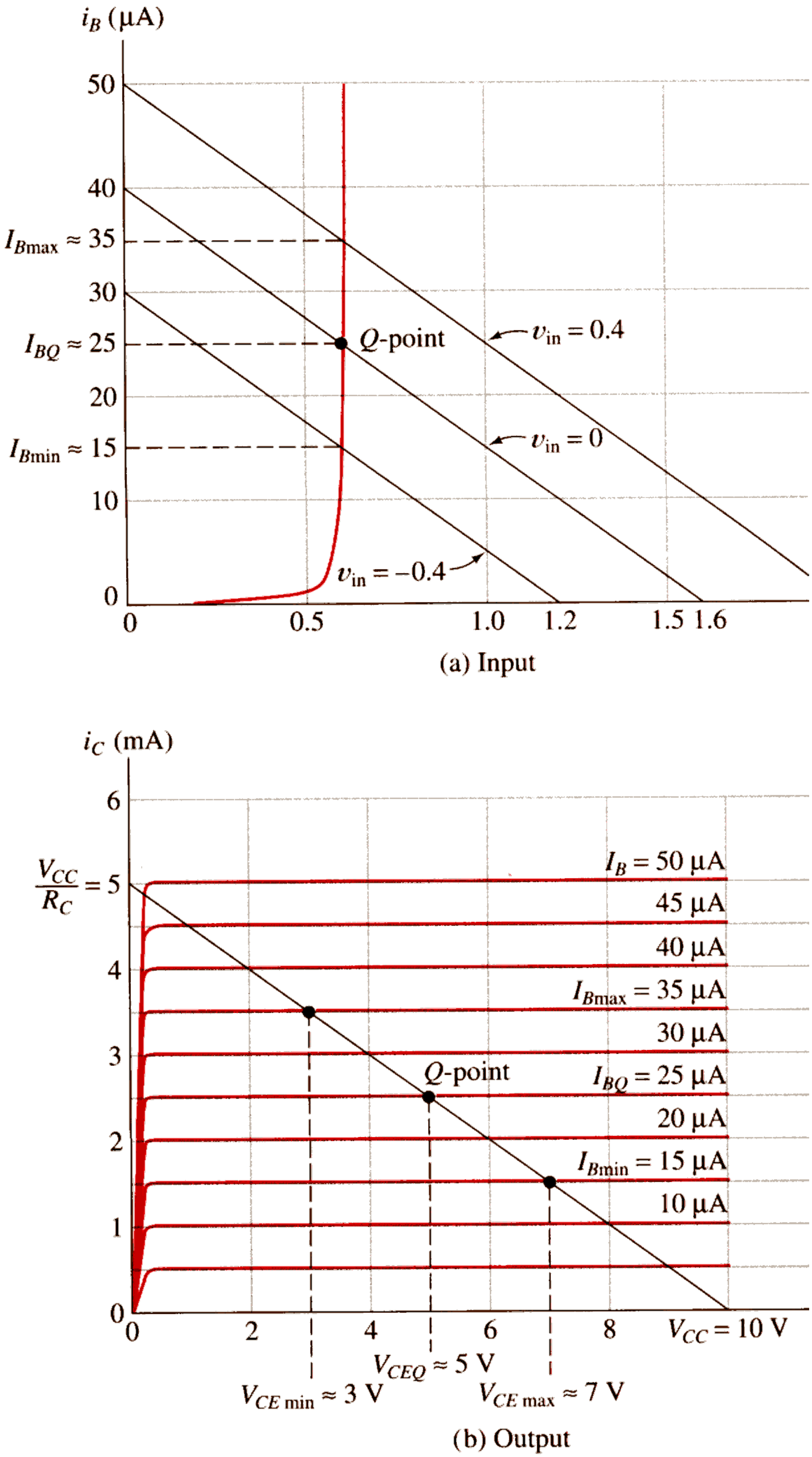
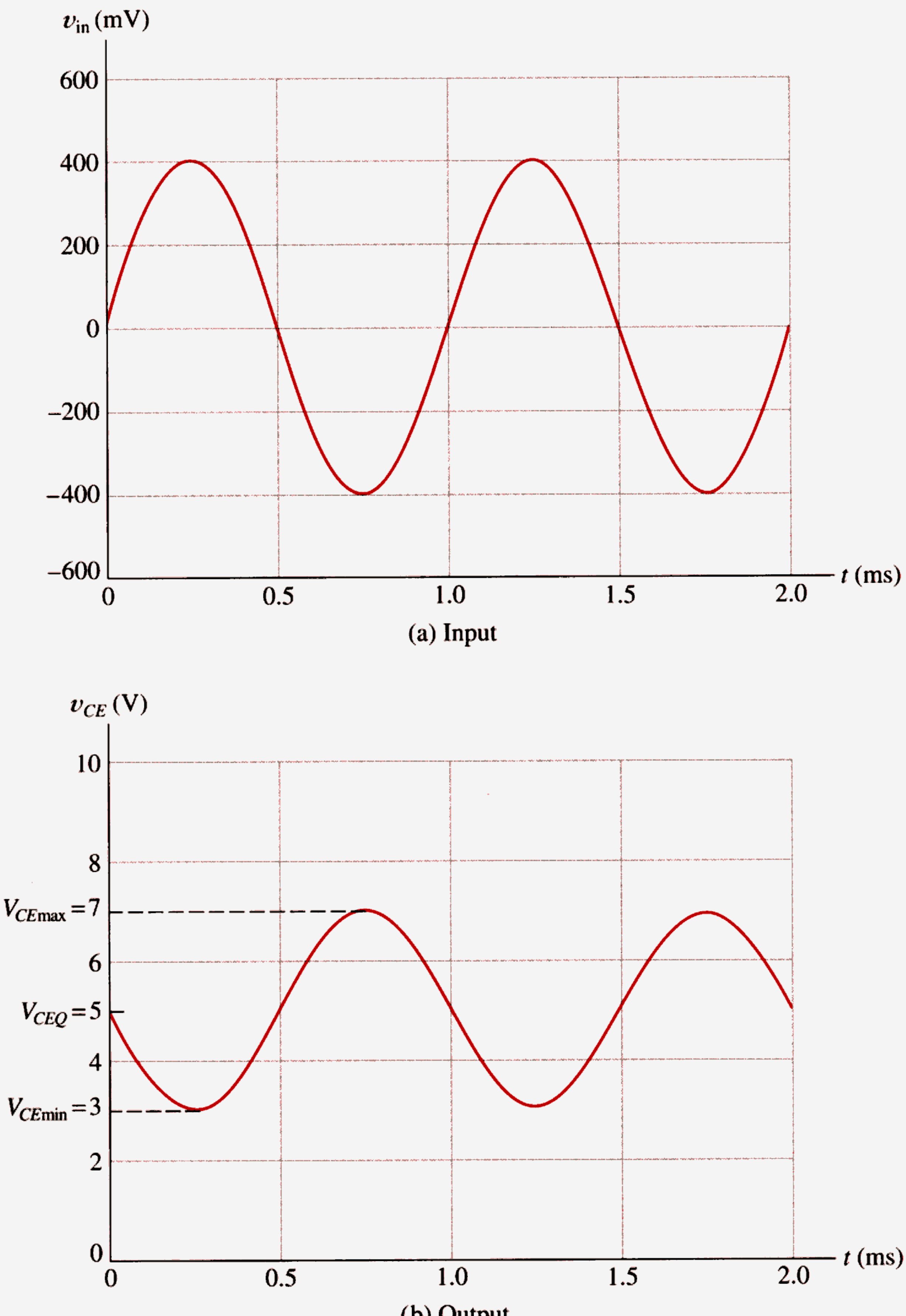


Figure 5.9 Load-line analysis for Example 5.2.

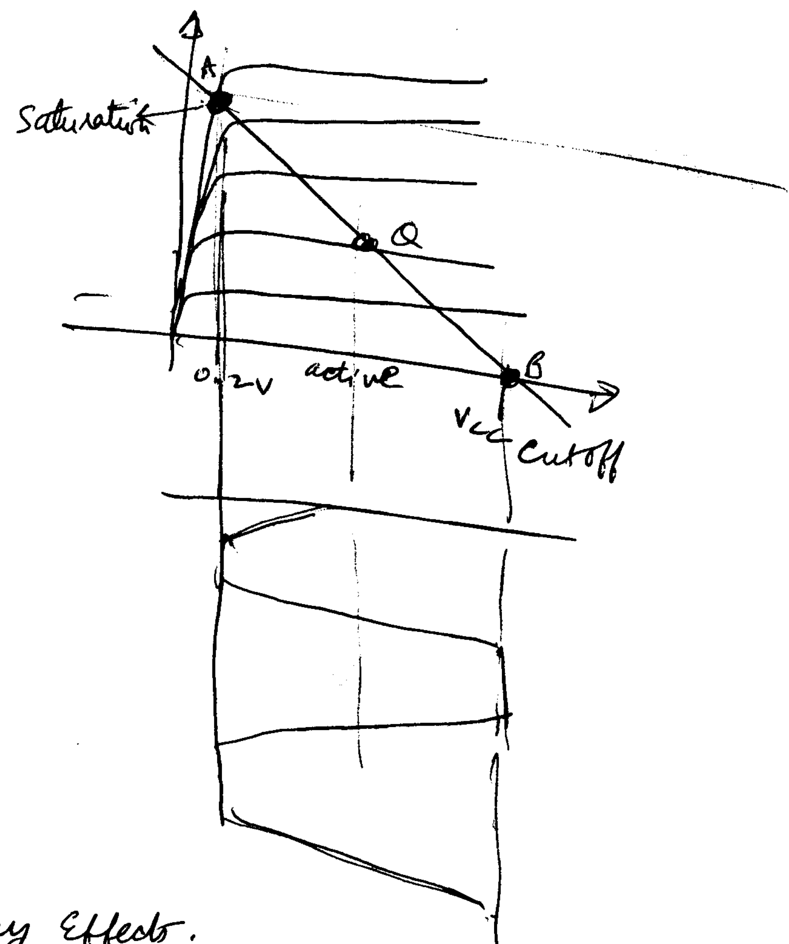


(a) Input

(b) Output

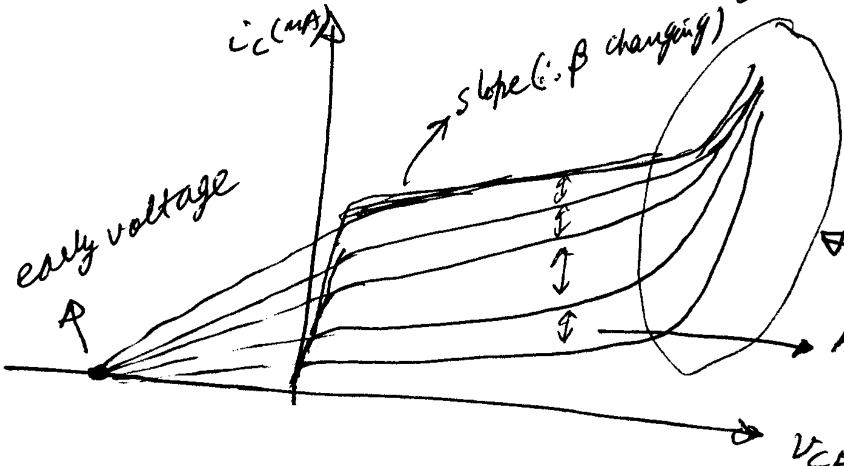
Figure 5.10 Voltage waveforms for the amplifier of Figure 5.7. See Example 5.2.

DISTORTION

- The output is not a <u>TRUE</u> sinusoid depending on the input/output characteristics of the amplifier (transistor).
- 

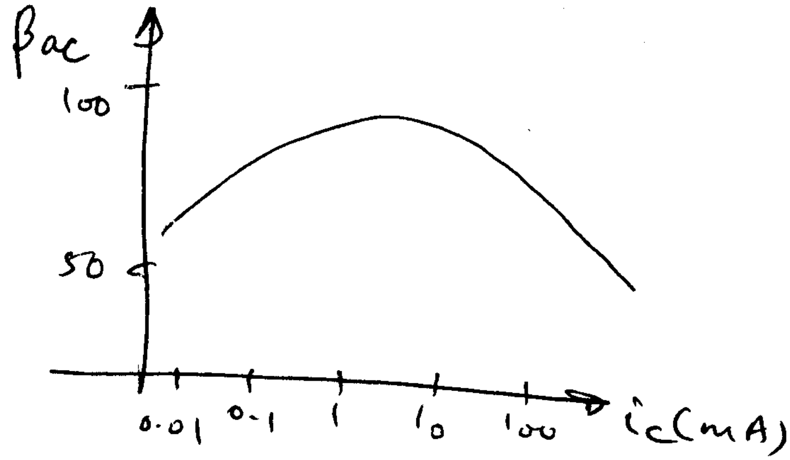
Secondary Effects:

Ideal model: First order model
Real BJTs show secondary effects.



collector Breakdown effect

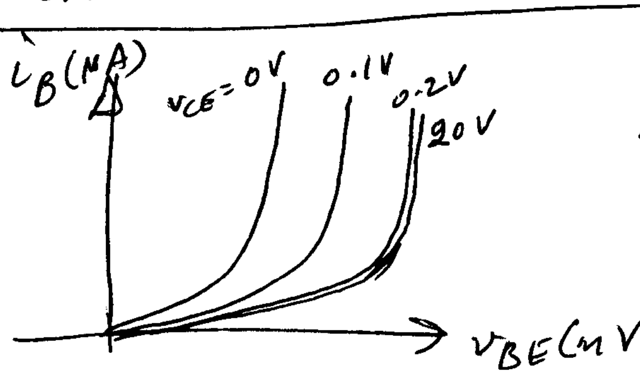
<u>ALSO</u>: β_{ac} changing due to non uniform spacing ($\beta_{ac} = \frac{\Delta i_c}{\Delta i_b}$)



- β also varies from unit to unit.
- Typically ratio of highest value to lowest value of $\beta = 3:1$
- β also varies with temperature
- β and β_{ac} also vary with i_C

Since β and β_{ac} ~~also~~ vary, therefore many times β and β_{ac} used interchangably; and also create designs which are insensitive to β variations.

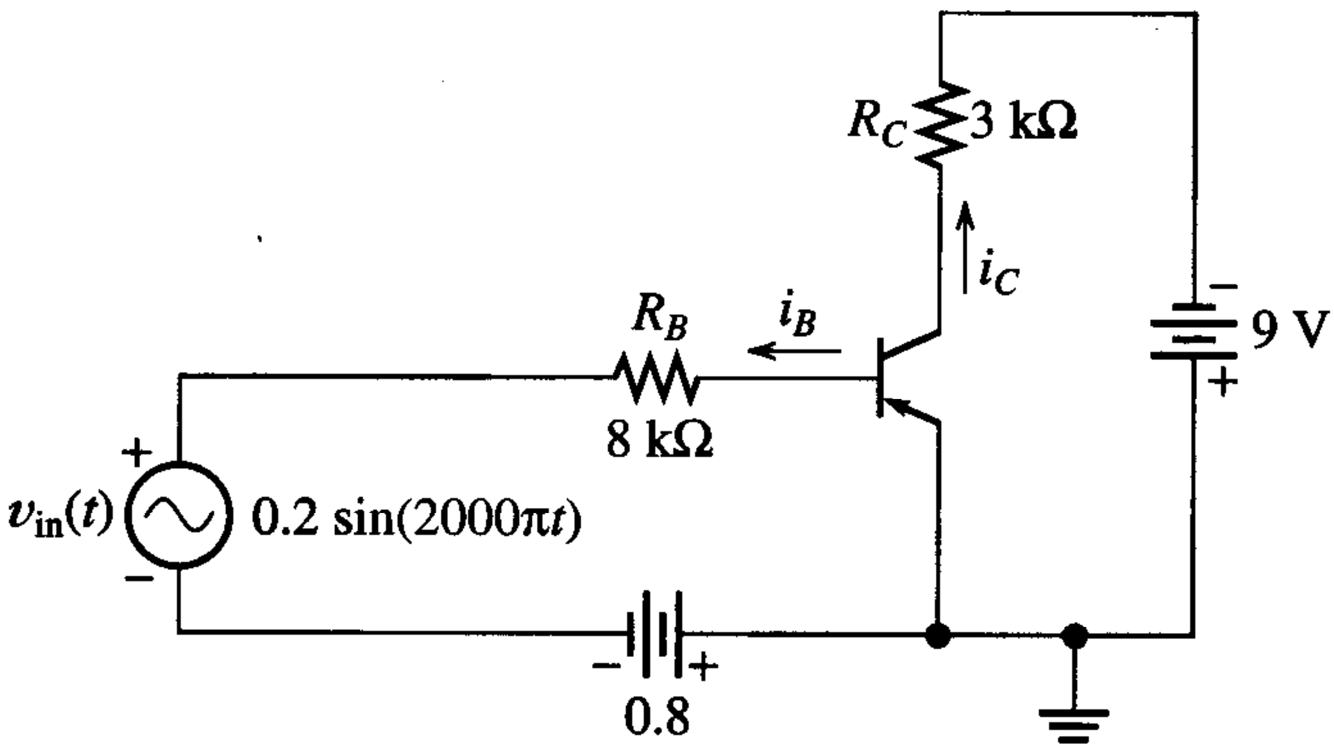
- <u>Input characteristics secondary effect</u>



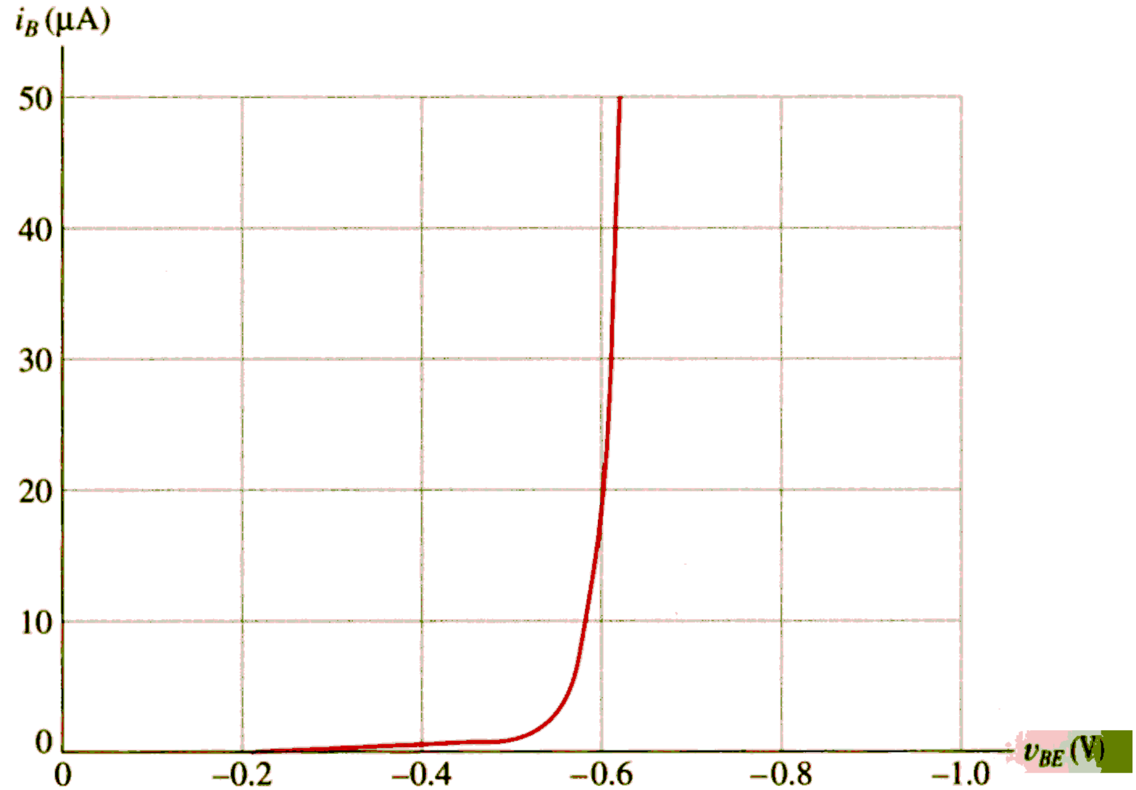
- Input curves change with V_{CE}.
- IF $V_{CE} > 0.2V$ (here) then practically same curve.

- <u>High Frequency (Charge Storage Effects)</u>

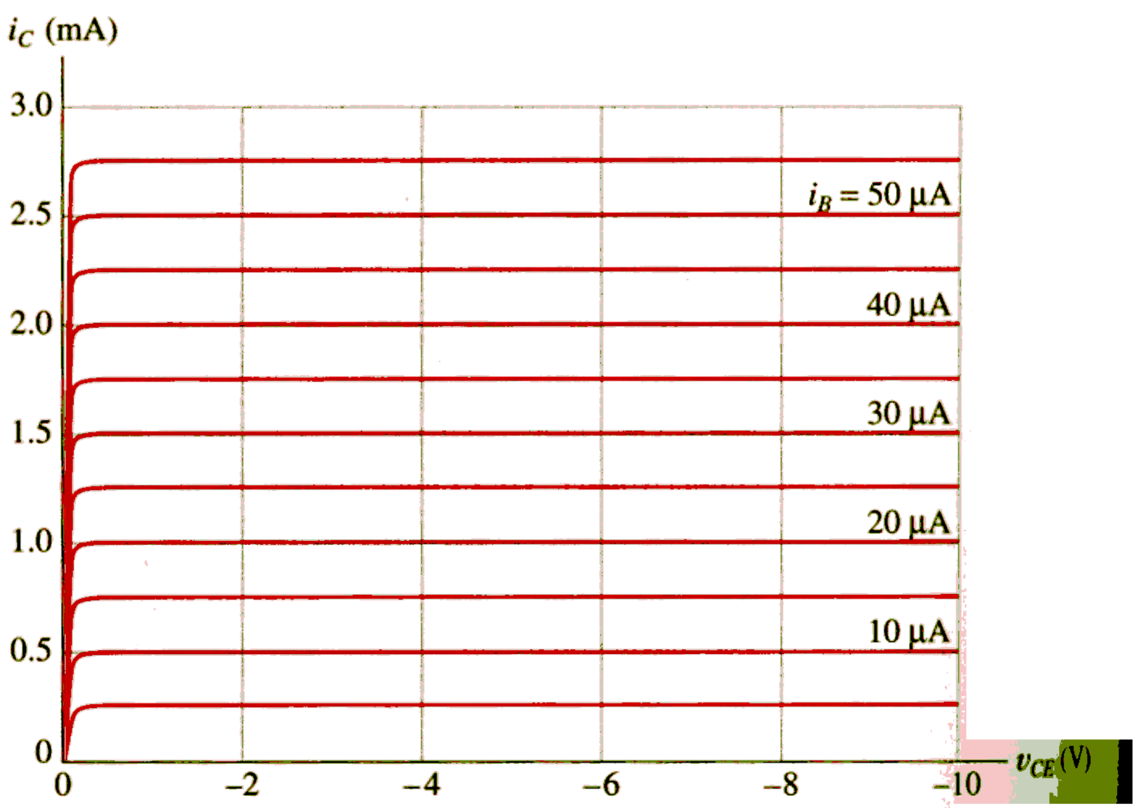
At high frequency we add capacitors in the BJT model (e.g between B and C, and B and E etc.)



Common-emitter amplifier using PNP



(a) Input



(b) Output

Common-emitter characteristics for a *pnp* BJT.

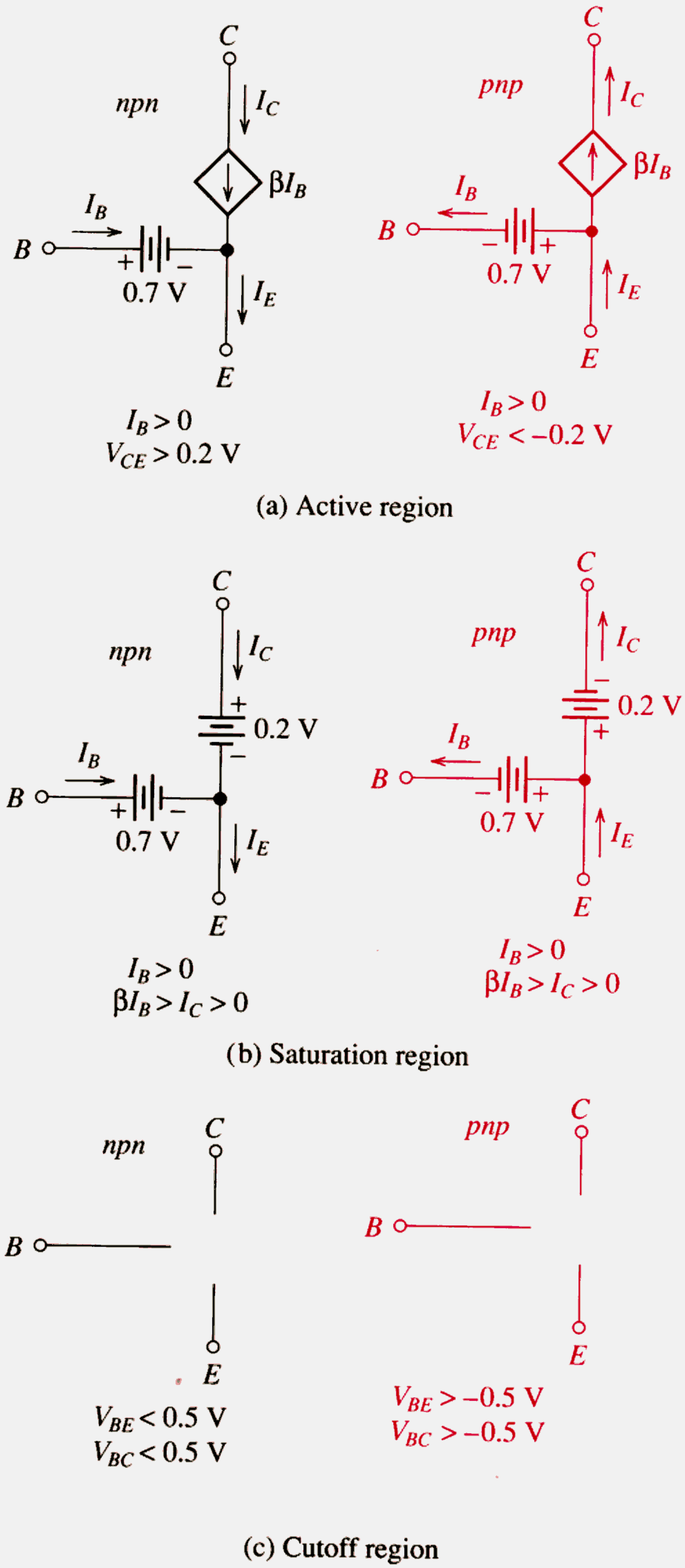
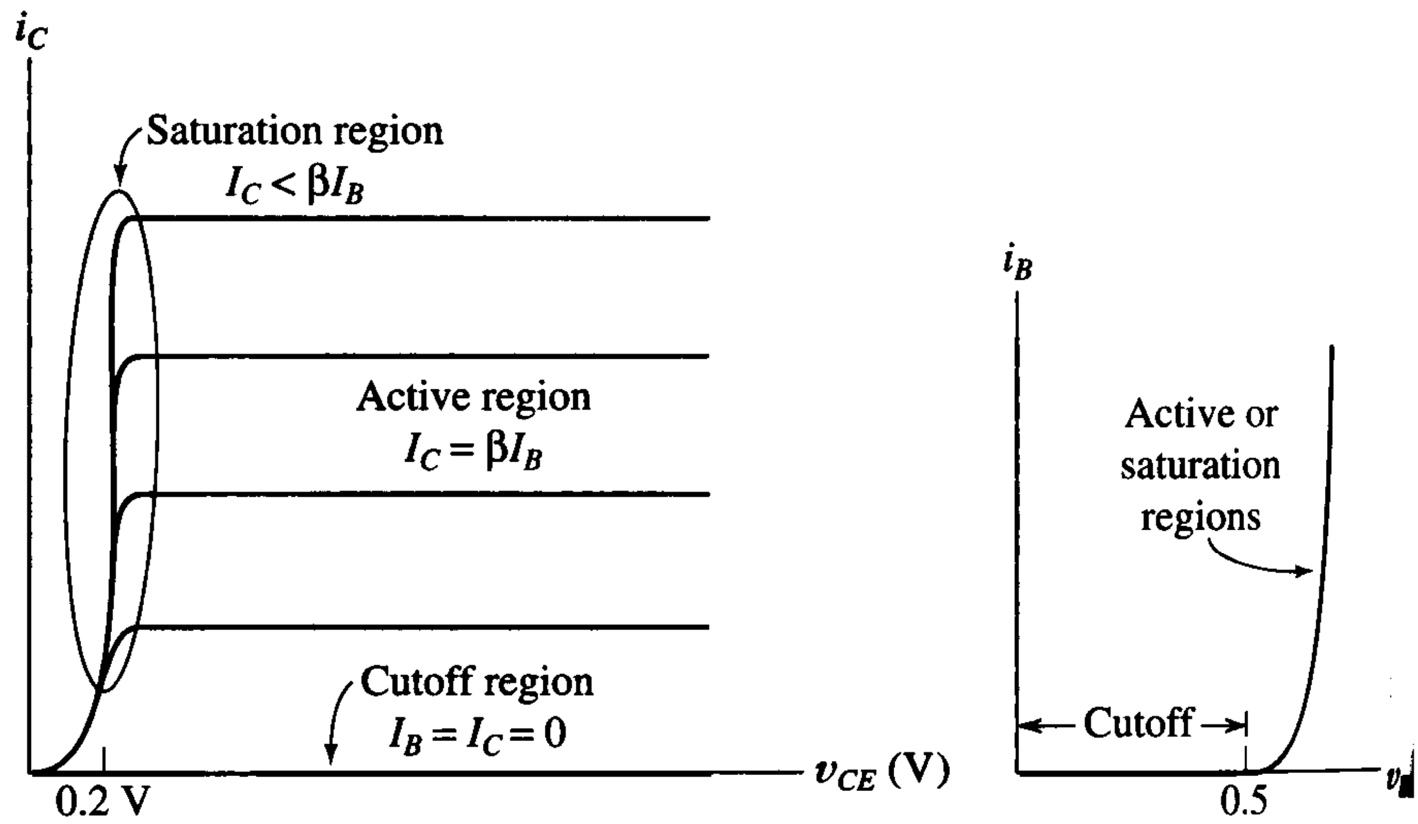


Figure 5.20
BJT large-signal models. (*Note:* Values shown are appropriate for typical small-signal silicon devices at a temperature of 300 K.)



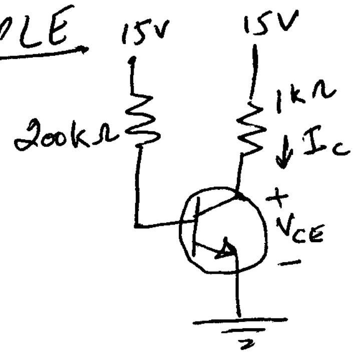
(a) Output characteristic

(b) Input characteristic

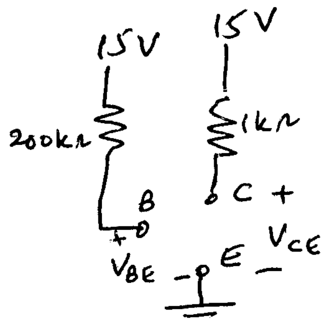
Large Signal DC Analysis

Just like Diode analysis assume a region of operation and then check for consistency.

EXAMPLE $\beta = 100$

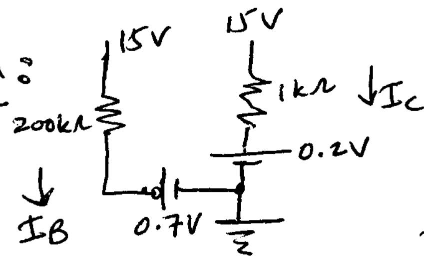


Assume: cutoff:



Here $V_{BE} = 15$
(for cutoff $V_{BE} < 0.5$)
$\therefore$ INCONSISTENCY

Saturation:

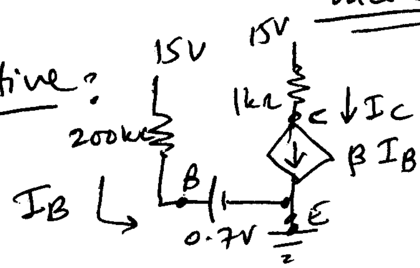


$$I_B = \frac{15-0.7}{200k\Omega} = 71.5\mu$$

$$I_C = \frac{15-0.2}{1k\Omega} = 14.8 \text{ mA}$$

Here $\beta I_B < I_C$ (should be $>$ for saturation)
inconsistent also

Active:



$$I_B = \frac{15-0.7}{200k\Omega} = 71.5\mu A$$

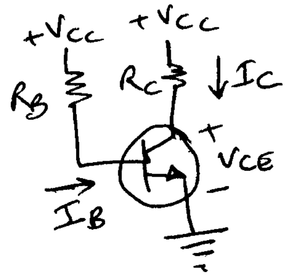
$$I_C = \beta I_B = 7.15 mA$$

$$V_{CE} = 15 - I_C(1k\Omega)$$
$$= 7.85V$$

$\therefore V_{CE} > 0.2V$ and $I_B > 0$

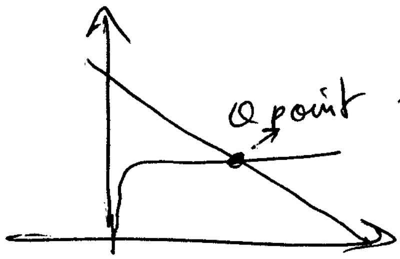
Transistor operate in ACTIVE region ✓

BASE BIAS

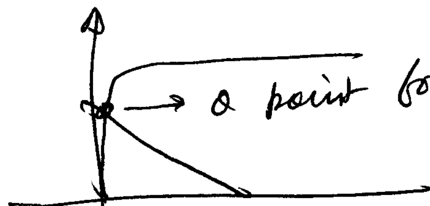


- I_B is controlled by V_{CC} and R_B
- Q point sensitive to changes in β

EXAMPLE 5.4 + 5.5

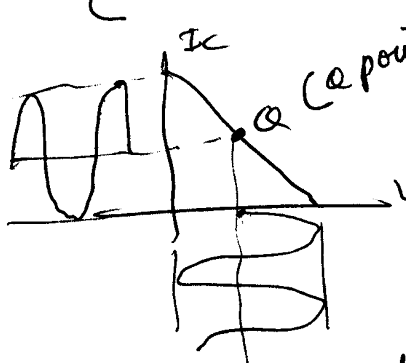


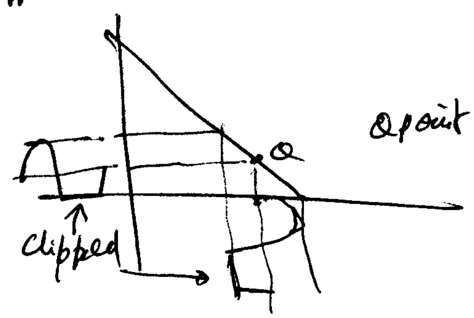
Q point for $\beta = 100$



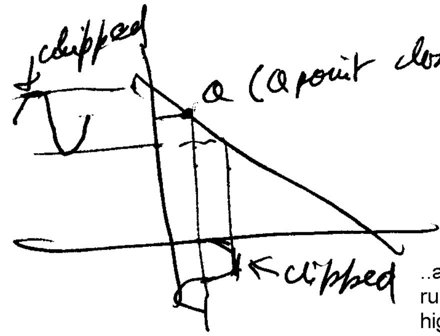
Q point for $\beta = 300$

- 1:3 variation is expected.
- Using this circuit, R_B would have to be adjusted to get Q in the middle (not practical)
- We need Q in the middle so that the AC signal can be amplified without distortion (CLASS A amplifiers)



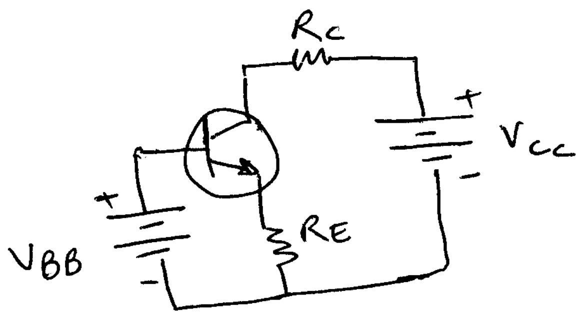


Q point close to cutoff

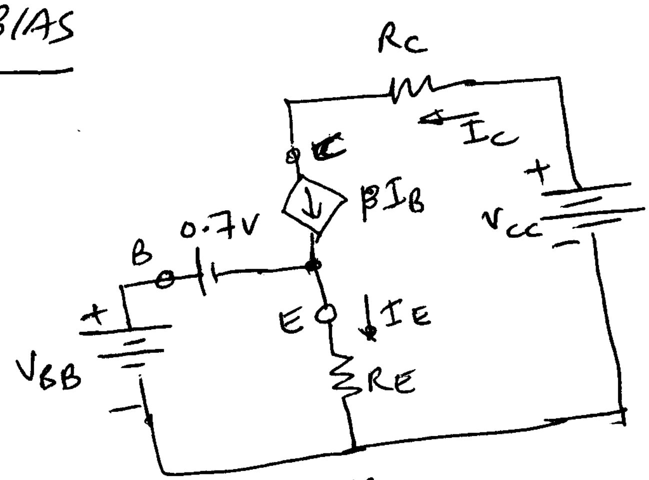


..also causes thermal runaway...because higher beta causes higher IC causing higher beta...

EMITTER BIAS



(A)



(B)

Assuming active region, we get (B) from (A)

$$V_{BB} = 0.7 + I_E R_E$$

$$\therefore I_E = \frac{V_{BB} - 0.7}{R_E} \quad \text{(Independent of } \beta\text{)}$$

$$I_C = \beta I_B \quad \text{and} \quad I_E = I_B + I_C$$

$$\therefore \quad I_E = (\beta+1) I_B$$

$$\therefore \quad I_B = \frac{I_E}{\beta+1}$$

$$\therefore I_C = \frac{\beta I_B}{(1+\beta)} \quad \text{(Fairly constant for high } \beta\text{)}$$

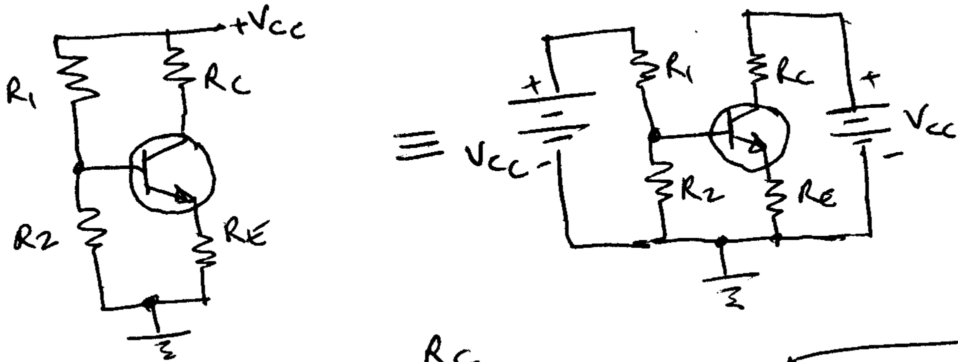
$$V_{CC} = R_C I_C + V_{CE} + R_E I_E$$

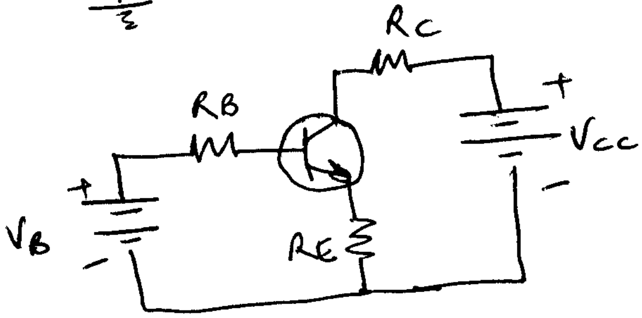
$$V_{CE} = V_{CC} - R_C I_C - R_E I_E \quad \text{(Fairly constant again because of } I_C\text{)}$$

NOT VERY PRACTICAL STILL

- Two sources required (V_{BB} and V_{CC})
- For AC signals the base is at ground ($\therefore$ doesn't allow AC signals to be fed at base).

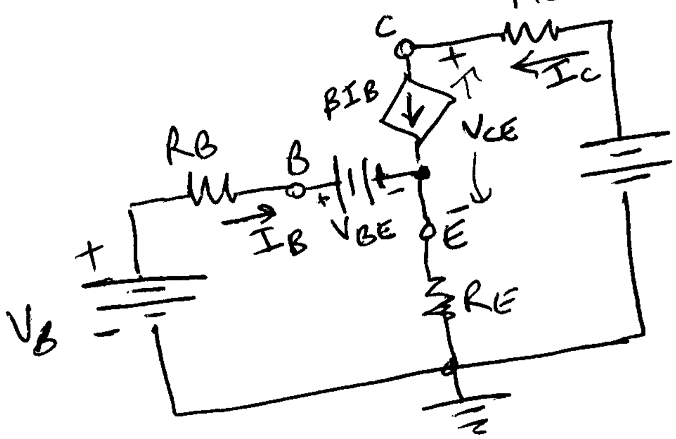
VOLTAGE DIVIDER BIAS





$$\boxed{V_B = \frac{R_2 V_{CC}}{R_1 + R_2}}$$

$$\boxed{R_B = \frac{1}{1/R_1 + 1/R_2} = R_1 \parallel R_2}$$



Usually $V_{BE} = 0.7\,V$

$$V_B = R_B I_B + V_{BE} + R_E I_E \quad \text{—} (1)$$

$$\because I_E = (\beta+1) I_B \quad \text{—} (2)$$

From (1) + (2) $\quad \therefore I_B = \dfrac{V_B - V_{BE}}{R_B + (\beta+1) R_E} \quad$ — (3)

$$V_{CE} = V_{CC} - R_C I_C - R_E I_E \quad \text{—} (4)$$

where $I_C = \beta I_B$ and $I_E = (\beta+1) I_B$ — (5)

use (3) in (4) using (5)

to solve for V_{CE}.

DESIGN CONSIDERATIONS FOR VOLTAGE DIVIDER BIAS

Recall

$$I_B = \frac{V_B - V_{BE}}{R_B + (\beta+1)R_E}$$

and $I_C = \beta I_B$ and $I_E = (\beta+1)I_B$

$\therefore$ If β is large and R_B is small

then
$$I_C = \beta I_B = \frac{\beta(V_B - V_{BE})}{(R_B + (\beta+1)R_E)}$$

$$\cong \frac{V_B - V_{BE}}{R_E} \text{ (independent of } \beta\text{)}$$

same for I_E ...

$\therefore$ $V_{CE} = V_{CC} - R_C I_C - R_E I_E$ (insensitive to β variations)

If R_B large, then I_C & V_{CE} vary with β.

So, keep R_1 and R_2 ~~large~~ small.

However, low R_1 and R_2 $\Rightarrow$ larger currents, overheating & need for larger (expensive) power supply.

$\therefore$ Compromise values of R_1 and R_2

- Choose R_2 so that current through R_2 = 10 (or 20 times) largest I_B expected.
- $\because$ $I_B = \dfrac{V_B - V_{BE}}{R_B + (\beta+1)R_E}$ and V_{BE} varies with temperature, make V_B larger than variations
- $V_B = \frac{1}{3}V_{CC}$; $V_{(\text{across } R_C)} = \frac{1}{3}V_{CC} = V_{(\text{across } R_E)} = V_{CE}$
- Use frequency response, peak signal swing, availability, cost etc. constraints also.

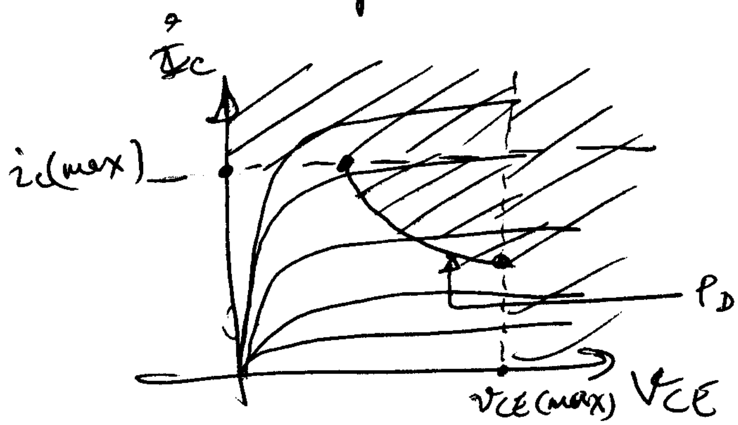
TRANSISTOR MAXIMUM RATINGS

Maximum ratings on

V_{EB}, V_{CB}, V_{CE} voltages

$I_C(max)$, $P_D(max)$ (Power)

$T_j(max)$ junction temperature



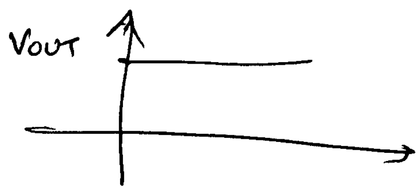
(ignoring power dissipate due to i_B)

$$T_j = T_A + \theta_{jA} P_D$$

junction temperature — ambient temperature — power dissipation

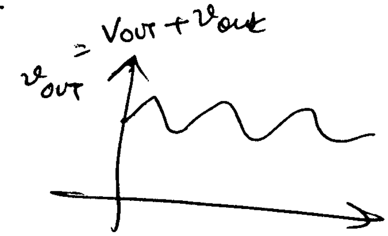
∴ of this $P_{D\,max}$ decreases with temperature.

BIAS & SIGNAL



DC BIAS

AC SIGNAL



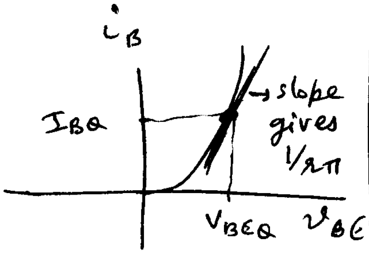
Composite

$$i_B(t) = I_{BQ} + i_b(t)$$
$$v_{BE}(t) = V_{BEQ} + v_{be}(t)$$
$$i_B = (1-\alpha) I_{ES}\left[\exp\left(\frac{v_{BE}}{V_T}\right) - 1\right]$$

in active region "1" is ignored

$$I_{BQ} + i_b(t) = (1-\alpha) I_{ES} \exp\left[\frac{V_{BEQ} + v_{be}(t)}{V_T}\right]$$
$$= \underbrace{(1-\alpha) I_{ES} \exp\left(\frac{V_{BEQ}}{V_T}\right)}_{I_{BQ}} \exp\left(\frac{v_{be}(t)}{V_T}\right)$$

ALTERNATE DERIVATION



$$\left.\frac{\partial i_B}{\partial v_{BE}}\right]_{I_{BQ}} = \frac{I_{BQ}}{V_T} = \frac{1}{r_\pi}$$

$\therefore$ $I_{BQ} + i_b(t) = I_{BQ} \exp\left(\frac{v_{be}(t)}{V_T}\right)$

Here v_{be} is very small, $\therefore$ using for $|x| \ll 1$, $\exp(x) = 1 + x$

$$I_{BQ} + i_b(t) \cong I_{BQ}\left(1 + \frac{v_{be}(t)}{V_T}\right)$$
$$i_b(t) = \frac{I_{BQ}}{V_T} v_{be}(t)$$

define $\boxed{\frac{V_T}{I_{BQ}} = r_\pi}$, then $\boxed{i_b(t) = \frac{v_{be}(t)}{r_\pi}}$

since $I_{BQ} = I_{CQ}/\beta \Rightarrow \boxed{r_\pi = \frac{\beta V_T}{I_{CQ}}}$

Typical value of $r_\pi = 2600\,\Omega$

Total current $i_C(t) = \beta i_B(t)$

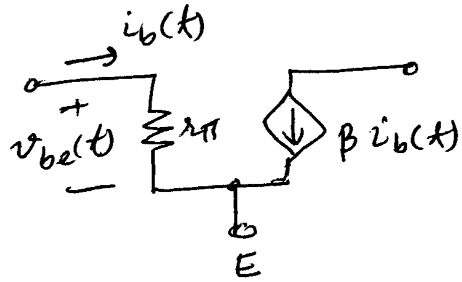
also $I_{CQ} = \beta I_{BQ}$

$\therefore$ $I_{CQ} + i_c(t) = \beta I_{BQ} + \beta i_b(t)$

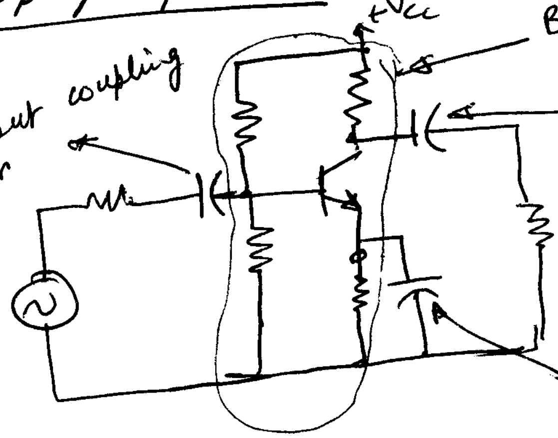
$\therefore$ $\boxed{i_c(t) = \beta i_b(t)}$

Small Signal Model for BJT

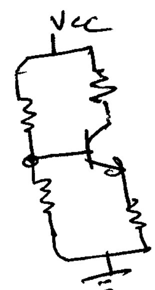
- Small signal model is EXACTLY the same for NPN and PNP.



- Coupling Capacitors.



For DC, capacitor is open,
∴ DC circuit is → which gives us Q point



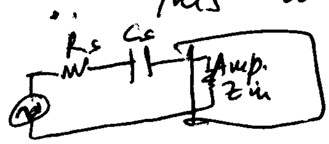
For AC, capacitor is a short
(also all DC sources are grounded).

Capacitor Impedance = ~~Xc~~ $-\dfrac{j}{\omega C}$ (= 0 at high frequency but large (∞) at low frequency

∴ If the signal has very low frequency then ~~the~~ capacitor is not a short, and at very high frequencies, the model for BJT is changed (additional capacitances added)

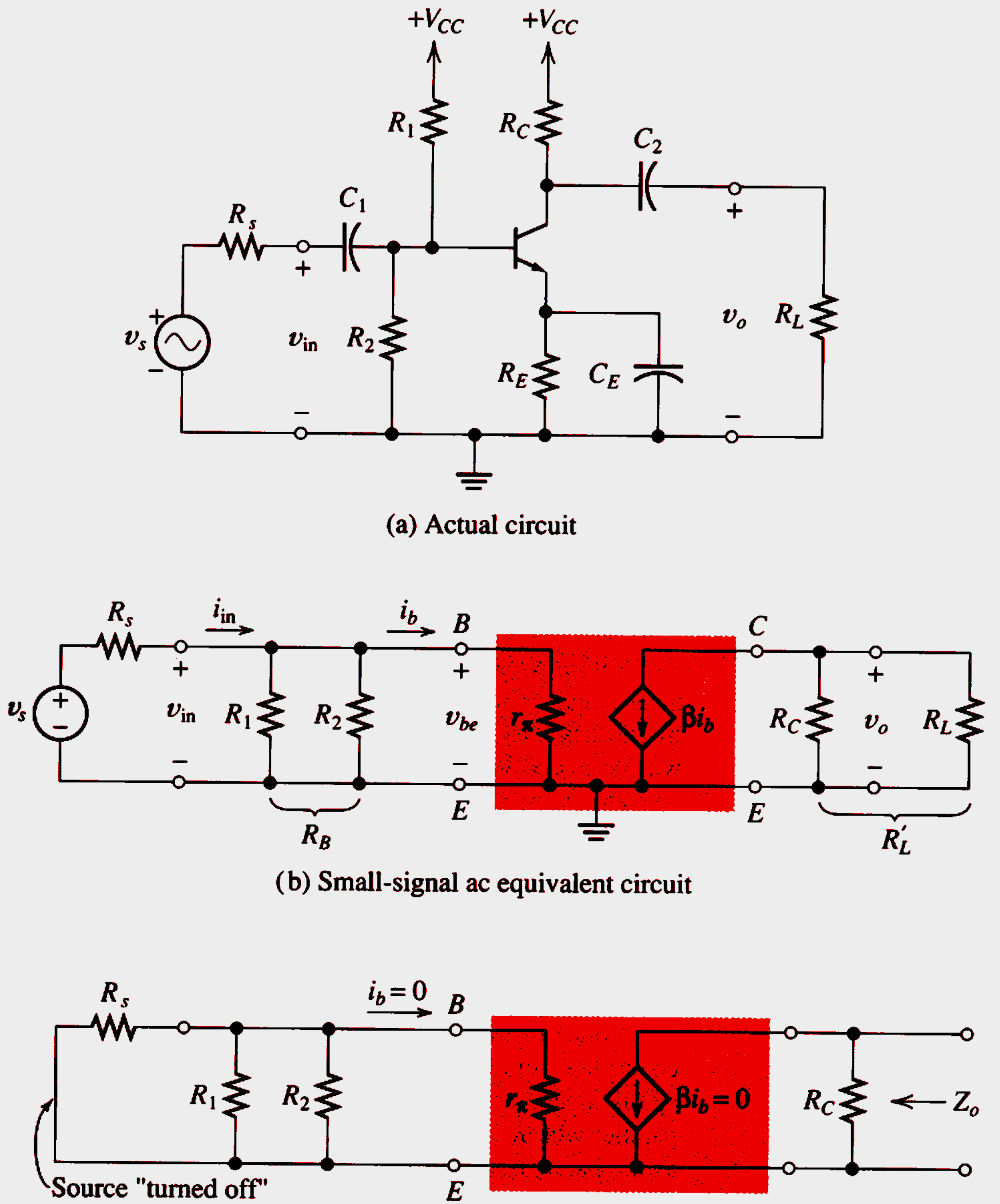
∴ This analysis true for $\boxed{\text{MID FREQUENCY RANGE}}$

For low impedance to AC ⟹



$X_C \le \dfrac{R_S + Z_{in}}{10}$

$X_{CO} \le \dfrac{R_L + Z_O}{10}$



(a) Actual circuit

(b) Small-signal ac equivalent circuit

(c) Equivalent circuit used to find Z_o

Figure 5.32 Common-emitter amplifier.

Common Emitter Amplifier (Small Signals)

VOLTAGE GAIN

$$v_{in} = v_{be} = i_b r_\pi$$

$$v_o = -R_L' \beta i_b$$

$$\therefore \; A_v = \frac{v_o}{v_{in}} = -\frac{\beta R_L'}{r_\pi}$$

$$\boxed{A_v = -\frac{\beta R_L'}{r_\pi}}$$

−ve sign to show inverting amplifier.

also $Av_o = -\frac{\beta R_c}{r_\pi}$ open circuit gain

LARGE VOLTAGE GAIN for Common Emitter.

INPUT IMPEDANCE

$$\boxed{Z_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{1/R_1 + \frac{1}{R_2} + \frac{1}{r_\pi}}}$$

CURRENT GAIN

$$\boxed{A_i = \frac{i_o}{i_{in}} = \frac{A_v Z_{in}}{R_L}}$$

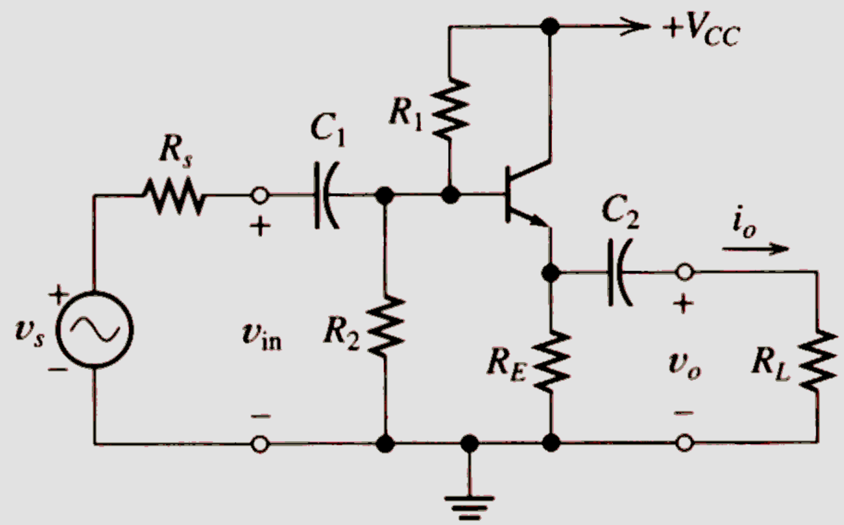
Power Gain

$$\boxed{G = A_i A_v}$$

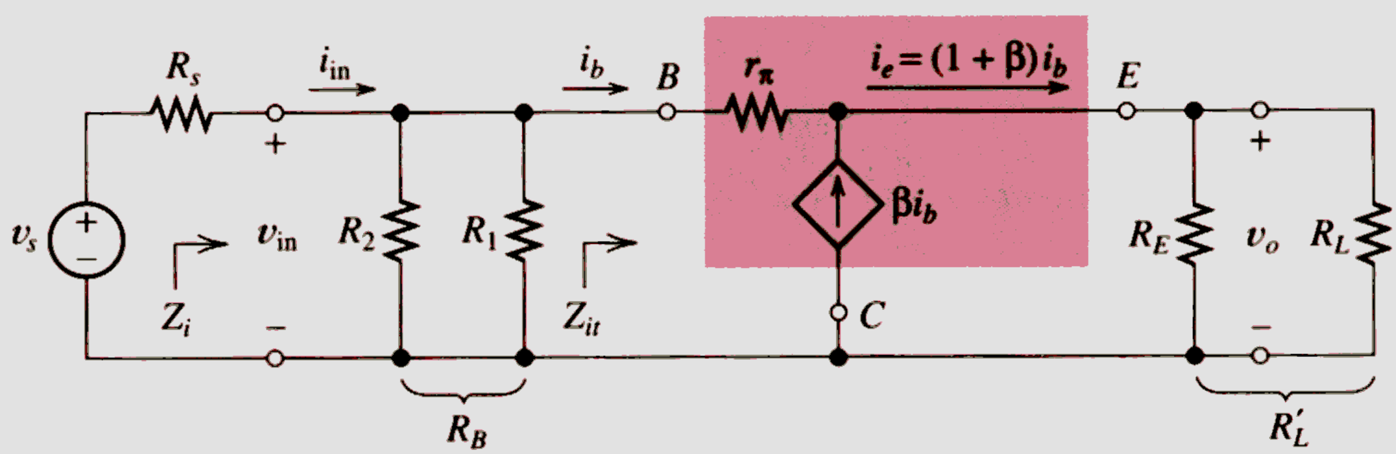
OUTPUT IMPEDANCE

set source voltage = 0 and then look at impedance from the output terminals.

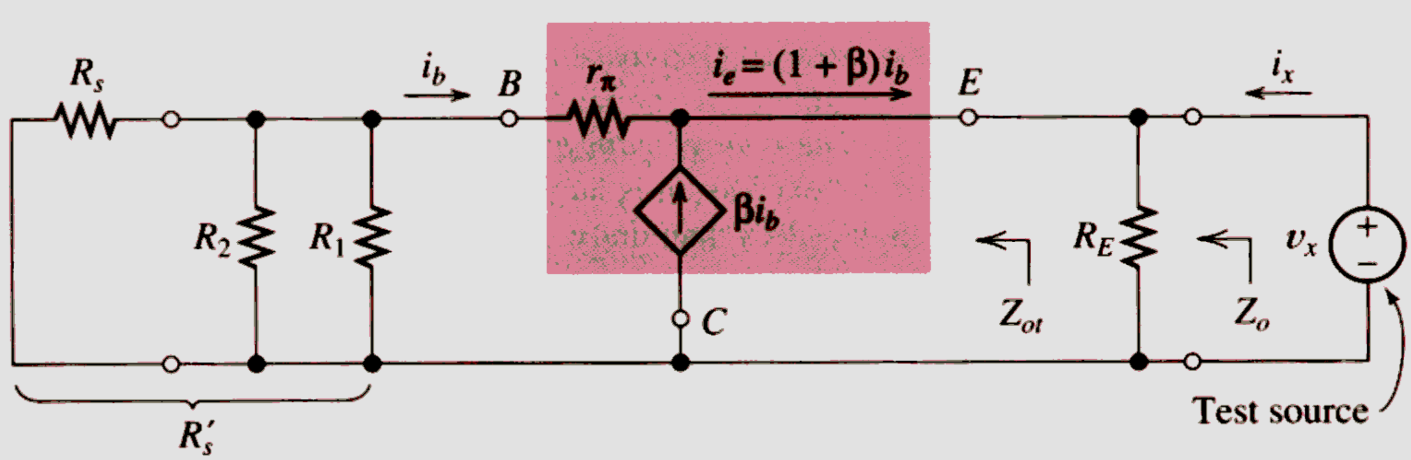
$$\boxed{Z_o = R_c}$$



(a) Actual circuit



(b) Small-signal equivalent circuit



(c) Equivalent circuit used to find output impedance Z_o

Figure 5.35 Emitter follower.

EMITTER FOLLOWER (Small Signal)

VOLTAGE GAIN

$$v_o = R_L'(1+\beta)i_b \quad -(1)$$

$$v_{in} = r_\pi i_b + (1+\beta) i_b R_L' \quad -(2)$$

$$\therefore \boxed{A_v = \frac{R_L'(1+\beta)}{r_\pi + (1+\beta)R_L'}} \quad -(3)$$

(notice $A_v < 1$) (close to 1)
- non inverting (follower)
- can provide current gain

INPUT IMPEDANCE

$$Z_i = \frac{1}{1/R_1 + 1/R_2 + 1/Z_{it}}$$

$$Z_{it} = \frac{v_{in}}{i_b} \text{ (use (2))} = \boxed{r_\pi + (1+\beta)R_L'} \quad -(4)$$

- Relatively high compared to other BJT configurations
- Can get higher using FET, and also using Feedback

OUTPUT IMPEDANCE

- Remove load
- turn off signal sources
- look in from output terminals

$$Z_o = \frac{v_x}{i_x} \quad -(5)$$

KCL at output node ⇒

$$i_b + \beta i_b + i_x = \frac{v_x}{R_E} \quad -(6)$$

define

$$R_s' = \frac{1}{1/R_s + 1/R_1 + 1/R_2} \quad -(7)$$

KVL at ~~output~~ outside loop all the way

$$v_x + r_\pi i_b + R_s' i_b = 0 \quad -(8)$$

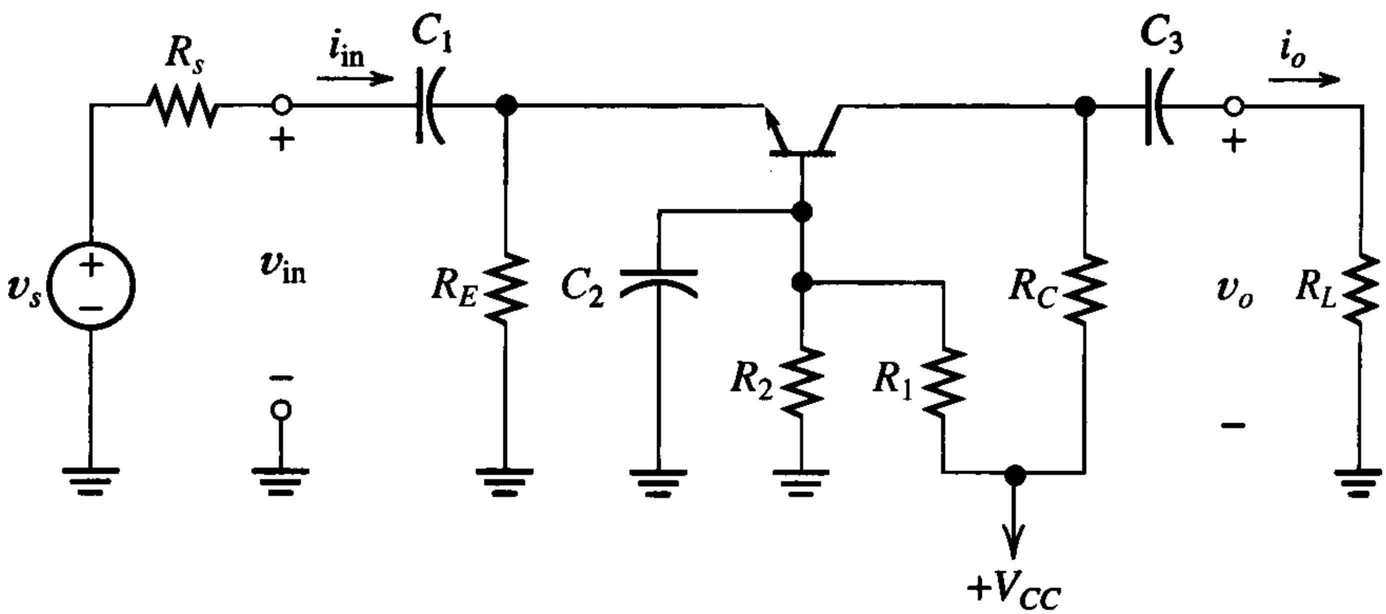
Replace i_b in (6) using (8) to get

$$Z_o = \frac{v_x}{i_x} = \frac{1}{\frac{(1+\beta)}{(R_s'+r_\pi)} + \frac{1}{R_E}} \quad -(9)$$

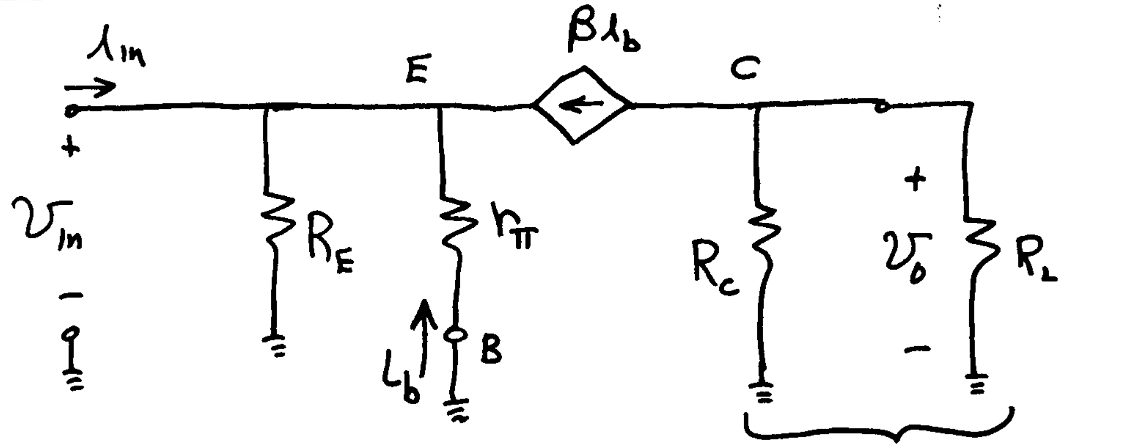
which is $Z_o = R_E \| Z_{ot}$

where $Z_{ot} = \dfrac{R_s' + r_\pi}{(1+\beta)}$

- Relatively low output impedance.



Common-base amplifier circuit.



$$R_L' = \frac{1}{1/R_C + 1/R_L}$$

$$v_{in} = -r_\pi i_b$$

$$v_o = -\beta i_b R_L'$$

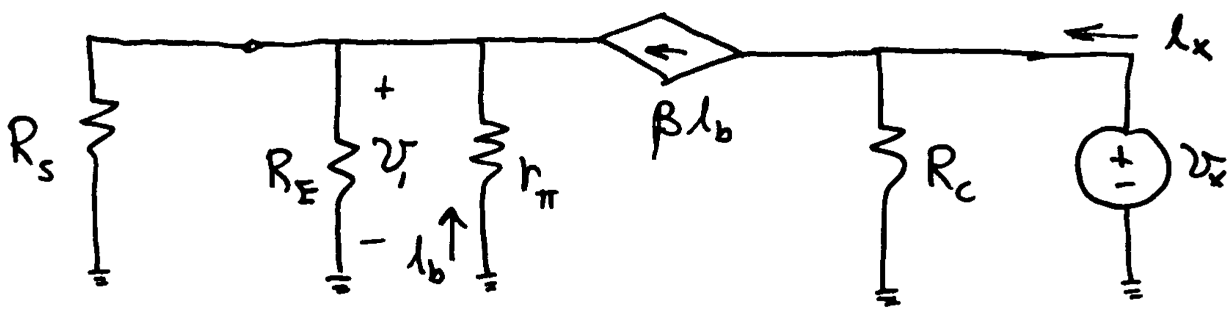
$$A_v = \frac{v_o}{v_{in}} = \frac{\beta R_L'}{r_\pi}$$

$$i_{in} = \frac{v_{in}}{R_E} - (\beta+1) i_b$$

$$i_{in} = \frac{v_{in}}{R_E} + \frac{\beta+1}{r_\pi} v_{in}$$

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{\frac{1}{R_E} + \frac{\beta+1}{r_\pi}}$$

Output resistance:



$$\left.\begin{aligned} \frac{v_1}{R_S} + \frac{v_1}{R_E} &= i_b + \beta i_b \\ v_1 &= -r_\pi i_b \end{aligned}\right\} \Rightarrow \quad i_b + \beta i_b + \frac{r_\pi}{R_S} i_b + \frac{r_\pi}{R_E} i_b = 0$$

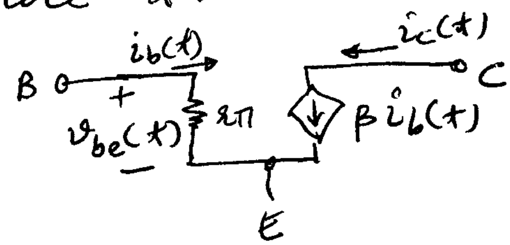
$$\therefore\ i_b = 0$$

$$R_o = \frac{v_x}{i_x} = R_C$$

SUMMARY (section 5.12)

- **Drawing Small Signal Equivalent Circuit**

  ① Replace dc voltage supply by a short.
  ② " " current " " open circuit.
  ③ For mid frequency analysis, replace capacitors by shorts.
  ④ Replace inductors by open circuit.
  ⑤ Replace transistor with its equivalent circuit.



← Transistor equivalent circuit

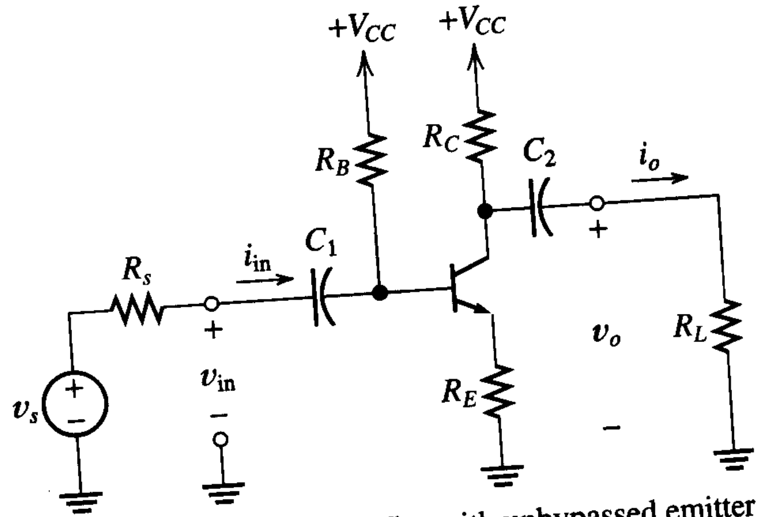
- Identify circuit variables of interest

- Finding output impedance
  ① Turn off <u>independent</u> sources (voltage + current; make them zero)
  ② Remove the load
  ③ Find impedance looking in from output terminals (might have to feed in test voltage V_x and then divide that by $\hat{i}_x$)

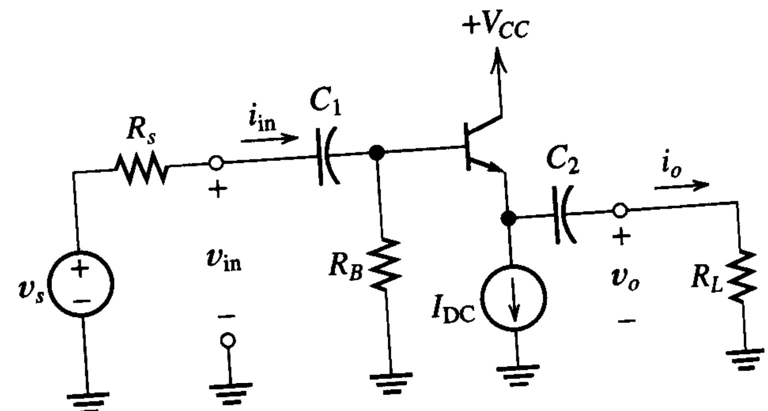
- Write circuit equations

- Find and check the desired expression

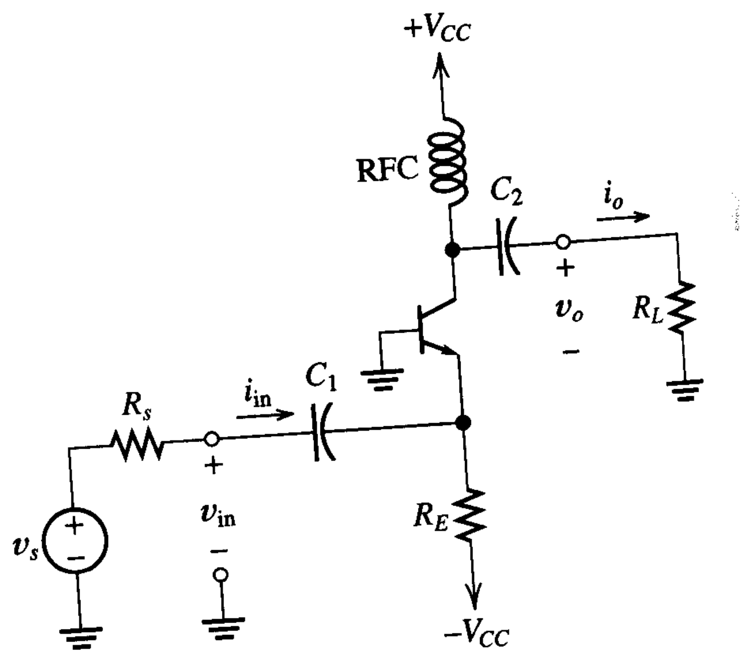
- Check units.



(a) Common-emitter amplifier with unbypassed emitter resistor



(b) Variation of the emitter follower using a dc current source for biasing



(c) Variation of the common-base amplifier [assume that the *radio-frequency choke* (RFC) is an open circuit for the ac signals]

Figure 5.40 Amplifier circuits.

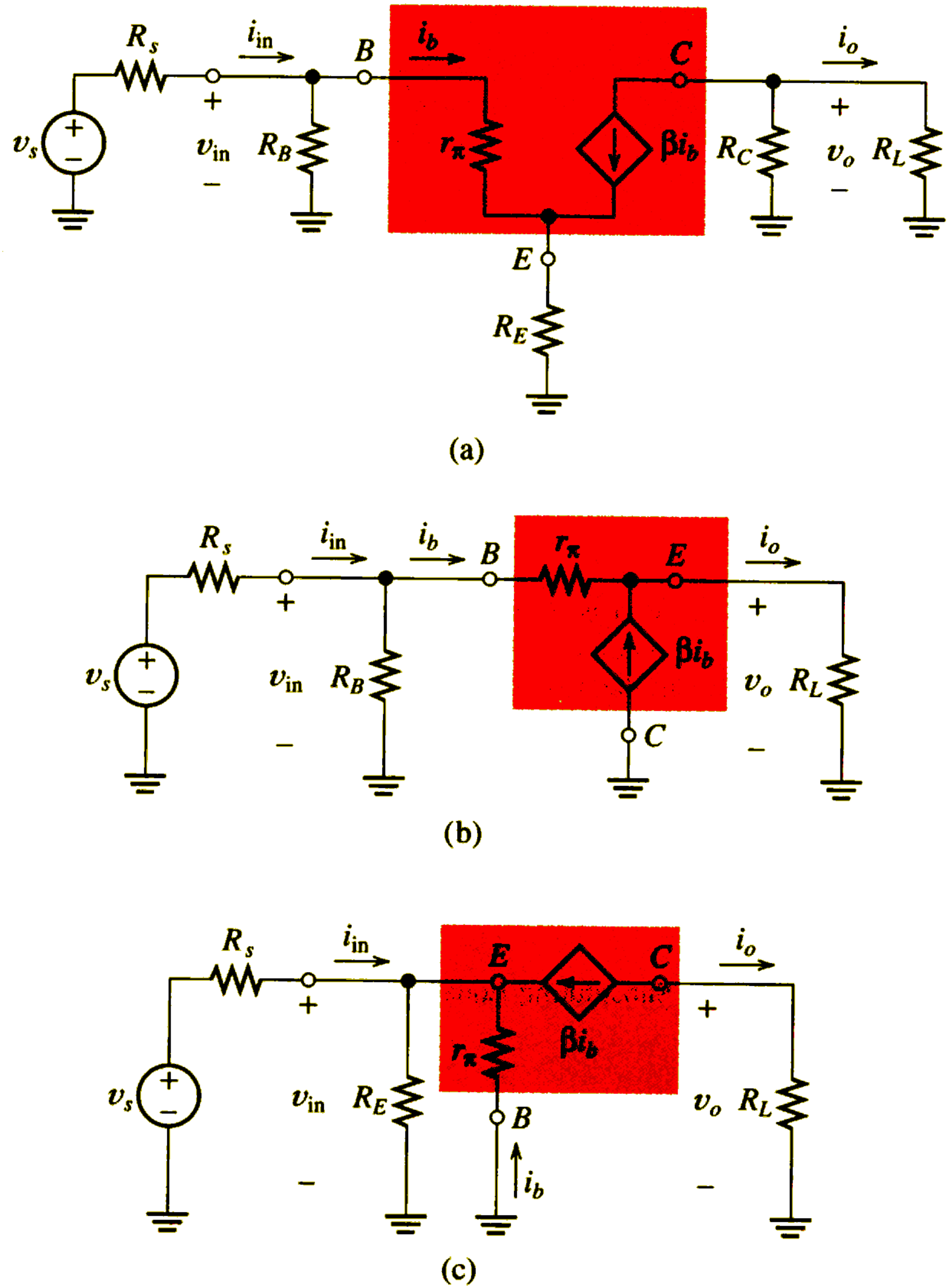
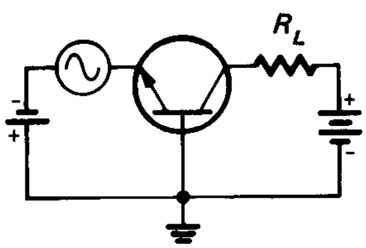
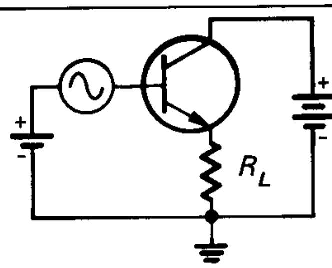
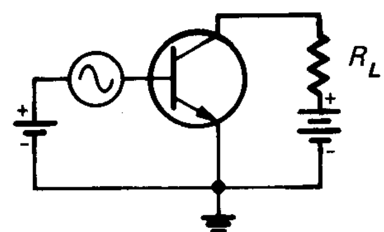
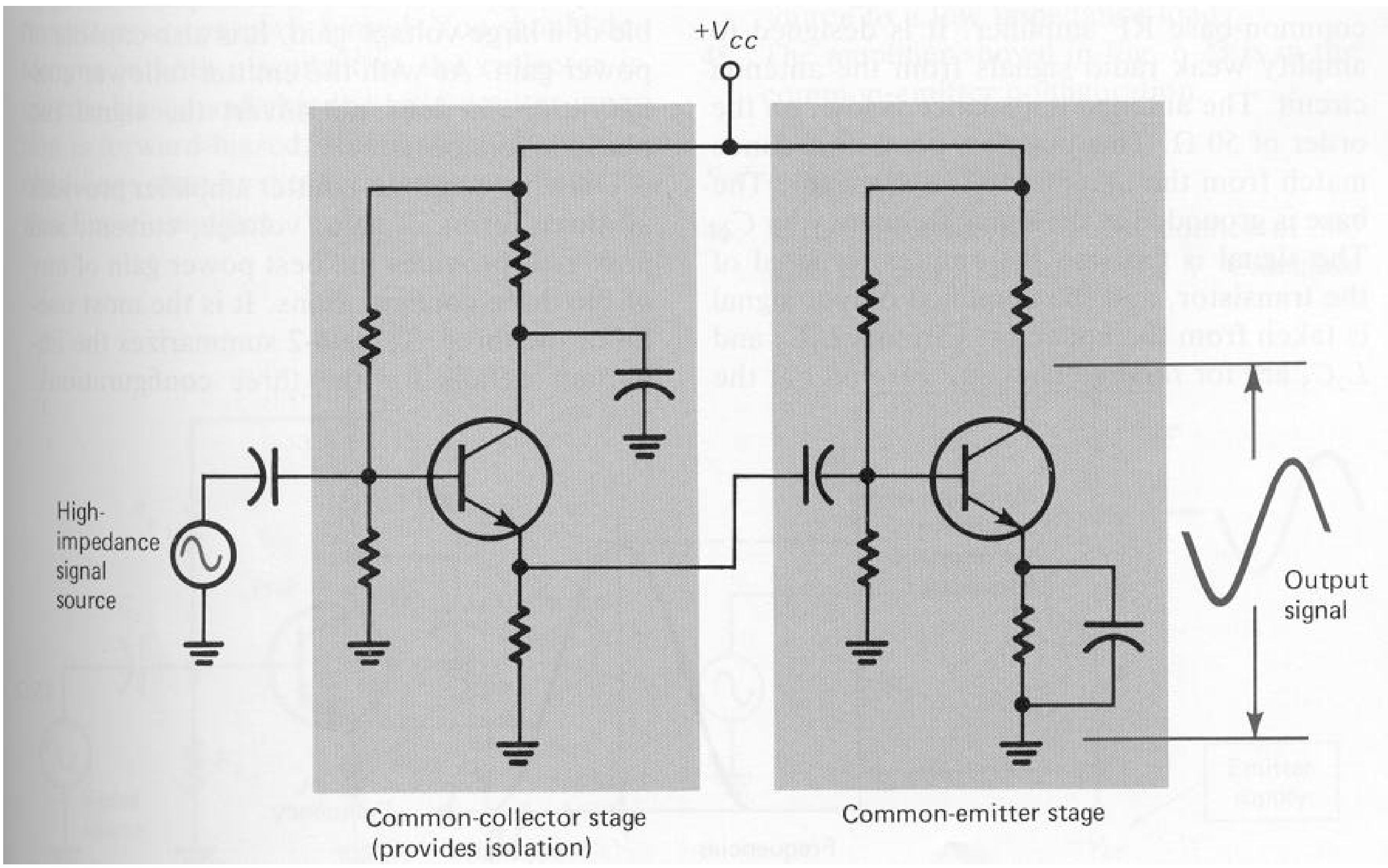


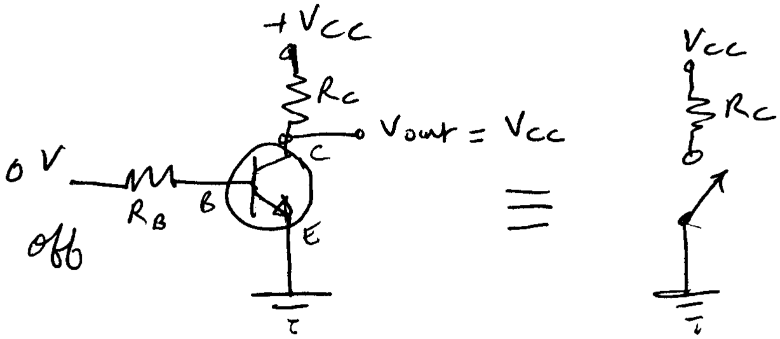
Figure 5.41 Small-signal equivalent circuits for the circuits of Figure 5.40.

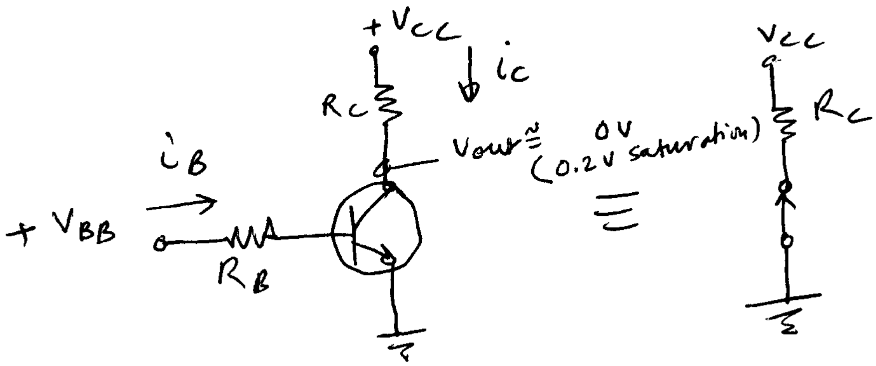
Summary of Amplifier Configurations

	Common Base	Common Collector	Common Emitter
Basic circuit (Showing signal source and load R_L)			
Power gain	Yes	Yes	Yes (highest)
Voltage gain	Yes	No (less than 1)	Yes
Current gain	No (less than 1)	Yes	Yes
Input impedance	Lowest (≈50 Ω)	Highest (≈300 kΩ)	Medium (≈1 kΩ)
Output impedance	Highest (≈1 MΩ)	Lowest (≈300 Ω)	Medium (≈50 kΩ)
Phase inversion	No	No	Yes
Application	Used mainly as an RF amplifier	Used mainly as an isolation amplifier	Universal—works best in most applications


+V_{CC}
High-impedance signal source
Output signal
Common-collector stage
(provides isolation)
Common-emitter stage

BJT as a SWITCH (or an Inverter)





$V_{out} = (V_{in})'$ (V_{out} = complement of V_{in})

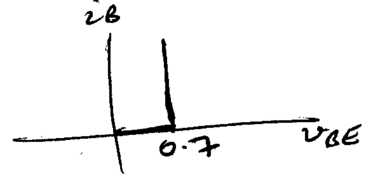
Condition in cutoff: $V_{CE} = V_{CC}$

Condition in Saturation:

$$i_{C(sat)} = \frac{V_{CC} - 0.2}{R_C} \quad \left(\text{Sometimes used as } \frac{V_{CC}}{R_C} \right)$$

Minimum Value of i_B needed for saturation: $\dfrac{i_{C(sat)}}{\beta}$

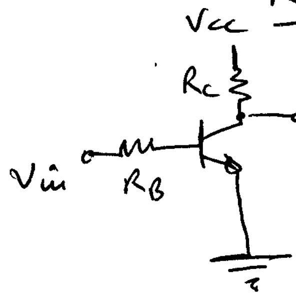
Equation to calculate i_B (using input characteristic as



)

$$\boxed{V_{BB} = i_B R_B + 0.7}$$

RTL logic (Inverter)



$V_o = V_{CC} - R_C i_C$

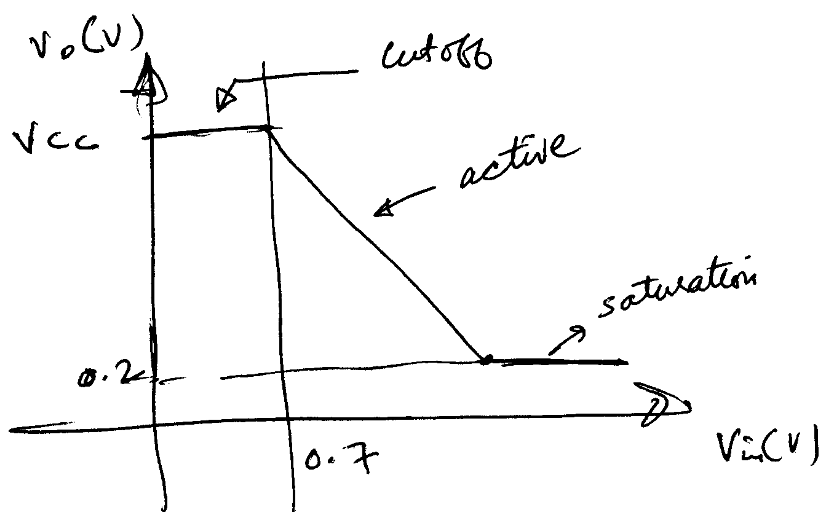
$i_C = \beta i_B$, $i_B = \dfrac{V_{in} - 0.7}{R_B}$

$\therefore \quad i_C = \beta \dfrac{V_{in} - 0.7}{R_B}$

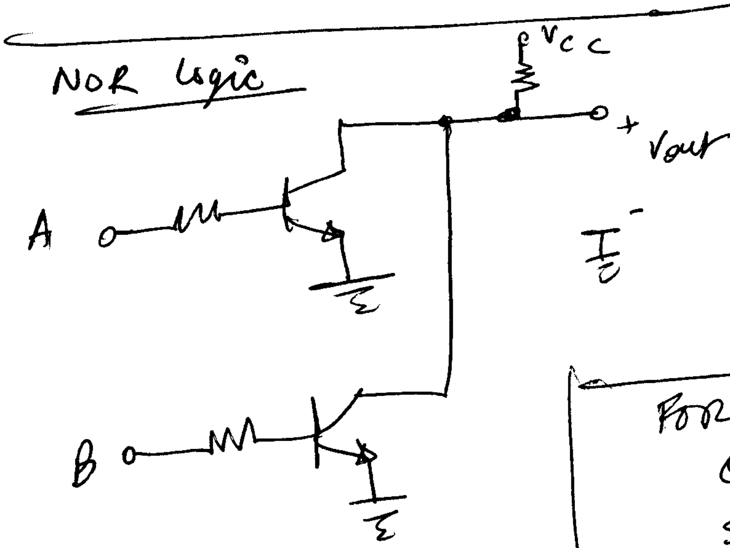
$$\boxed{V_o = V_{CC} - R_C \beta \frac{V_{in} - 0.7}{R_B}} \quad -(1)$$

If $V_o < 0.2$, then $V_o = 0.2$ (saturation)
(using (1))

If $V_{in} < 0.7$ then $V_o = V_{CC}$
(cutoff)

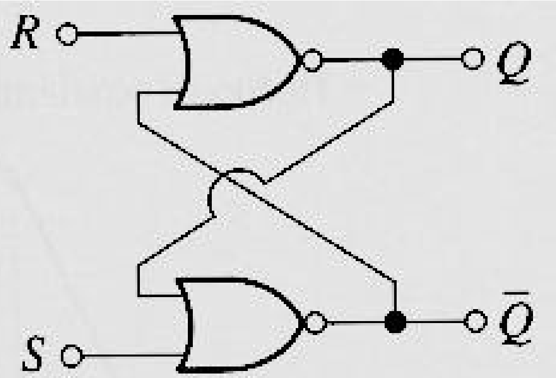


NOR logic

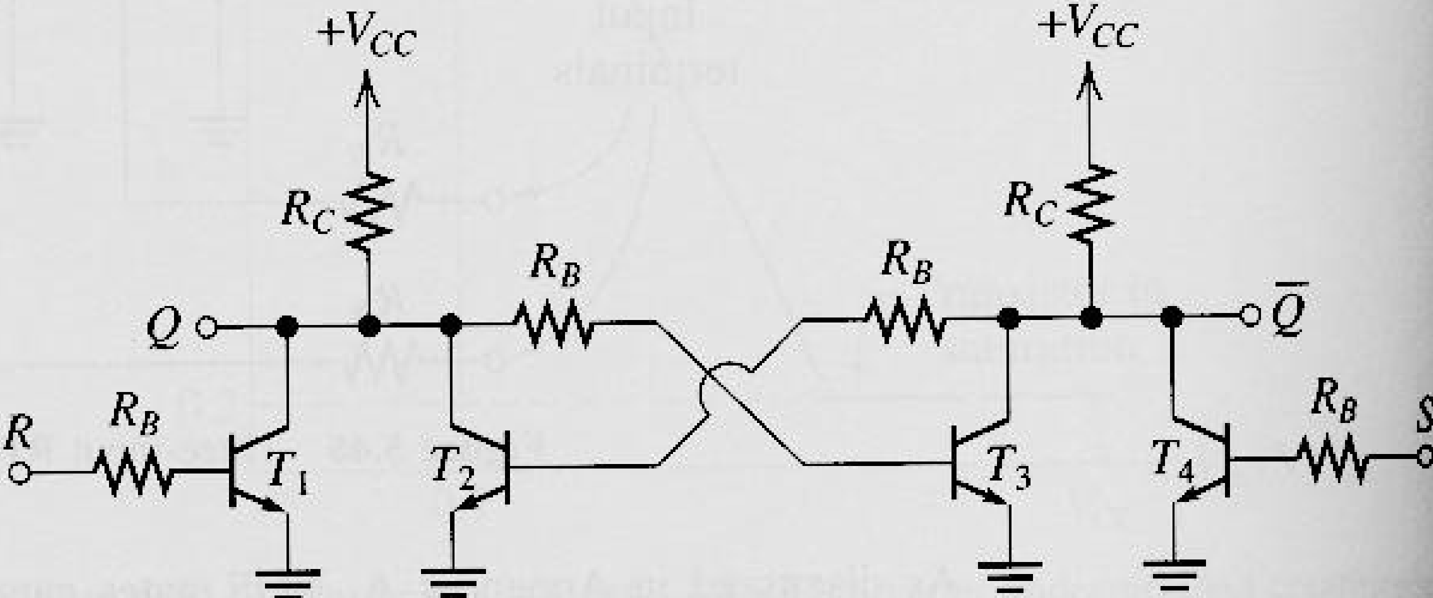


A	B	Vout
0	0	1
0	1	0
1	0	0
1	1	0

FOR FLIP FLOP
Q and $\bar{Q}$ opposite logic
S ⇒ Q = 1, R ⇒ Q = 0
(S, R) = (0, 0) keep previous state
(S, R) = (1, 1) NOT ALLOWED.



(a) Logic diagram



(b) RTL circuit diagram

Figure 5.47 *RS* flip-flop.