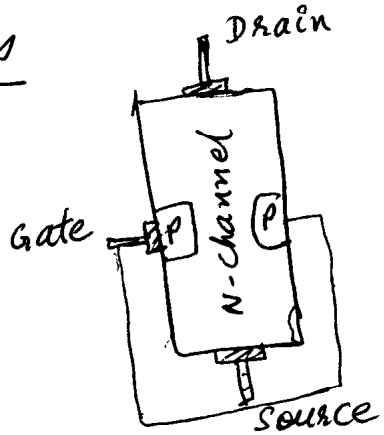
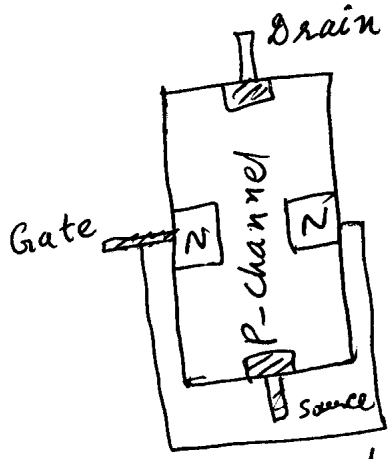
JUNCTION FIELD EFFECT TRANSISTOR (JFET)

- **Types**

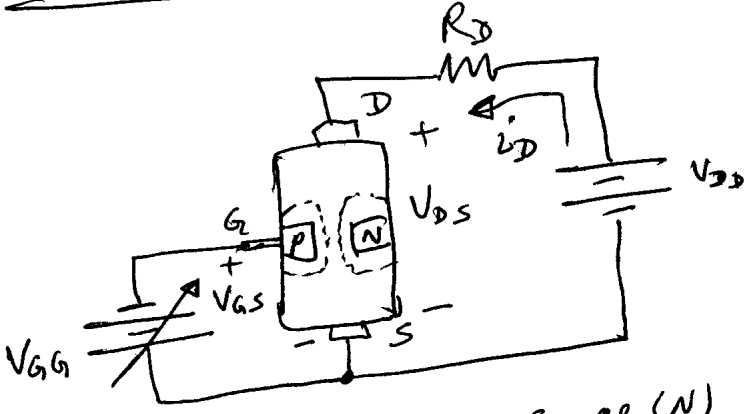


N-channel JFET



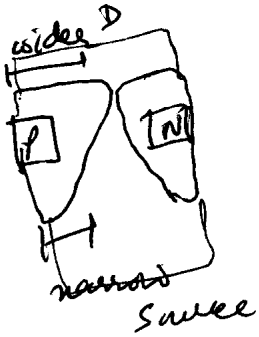
P-channel JFET

- **Basic Operation**

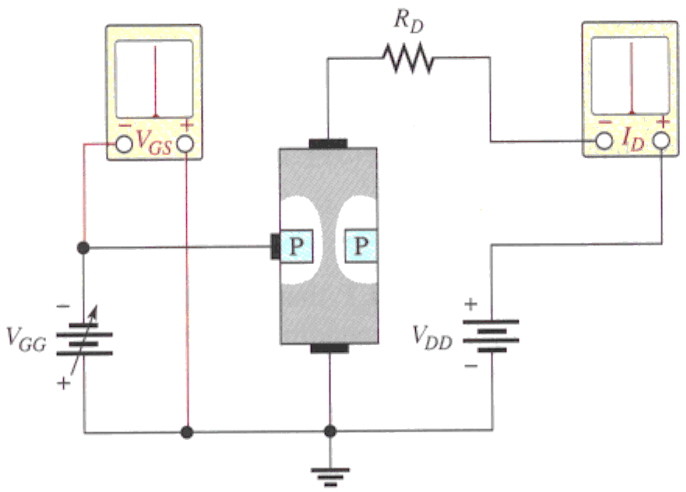


- Gate (P) and source (N) are kept reverse biased.
- By increasing the magnitude of V_{GS} (i.e V_{GG}) the depletion layer increase which increases the channel resistance, hence decreasing i_D.

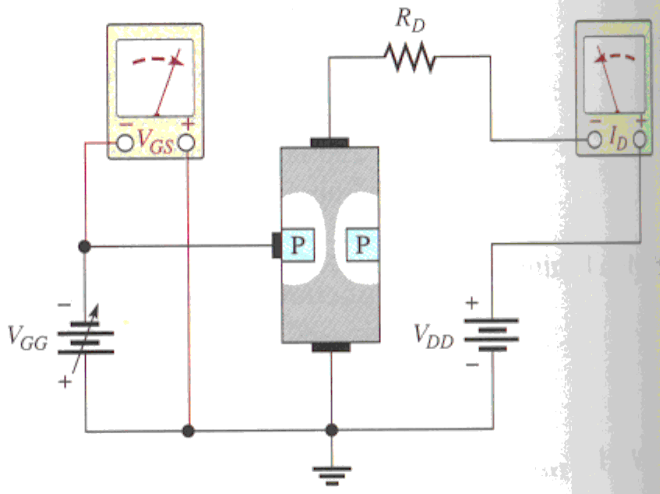
$\therefore$ **V_{GS} controls i_D**



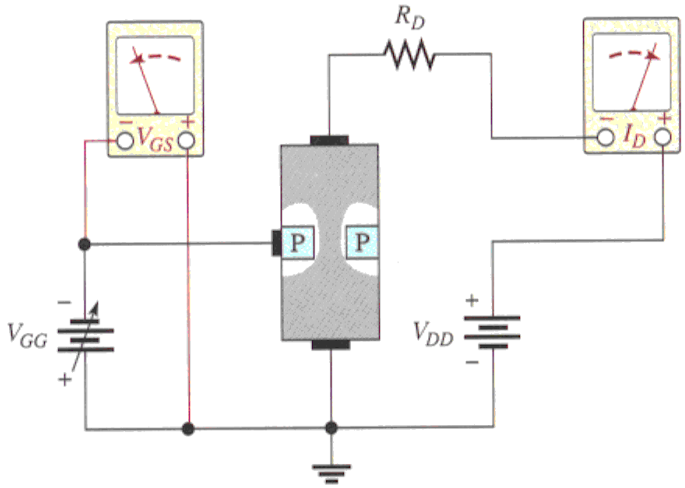
the drain side of depletion layer is wider $\because$ there is more reverse bias on G and D is greater than that on G and S.



(a) JFET biased for conduction



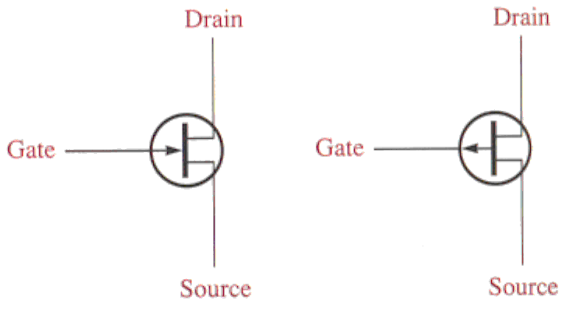
(b) Greater V_{GG} narrows the channel, thus decreasing I_D.



(c) Less V_{GG} widens the channel and increases I_D.

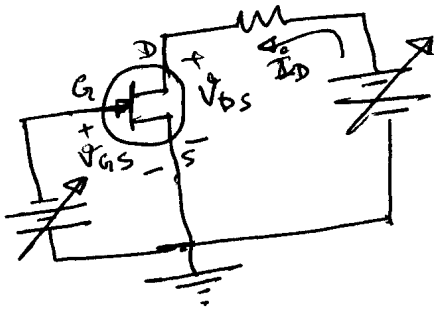
FIGURE 18–27
Effects of V_{GG} on channel width and drain current ($V_{GG} = V_{GS}$).

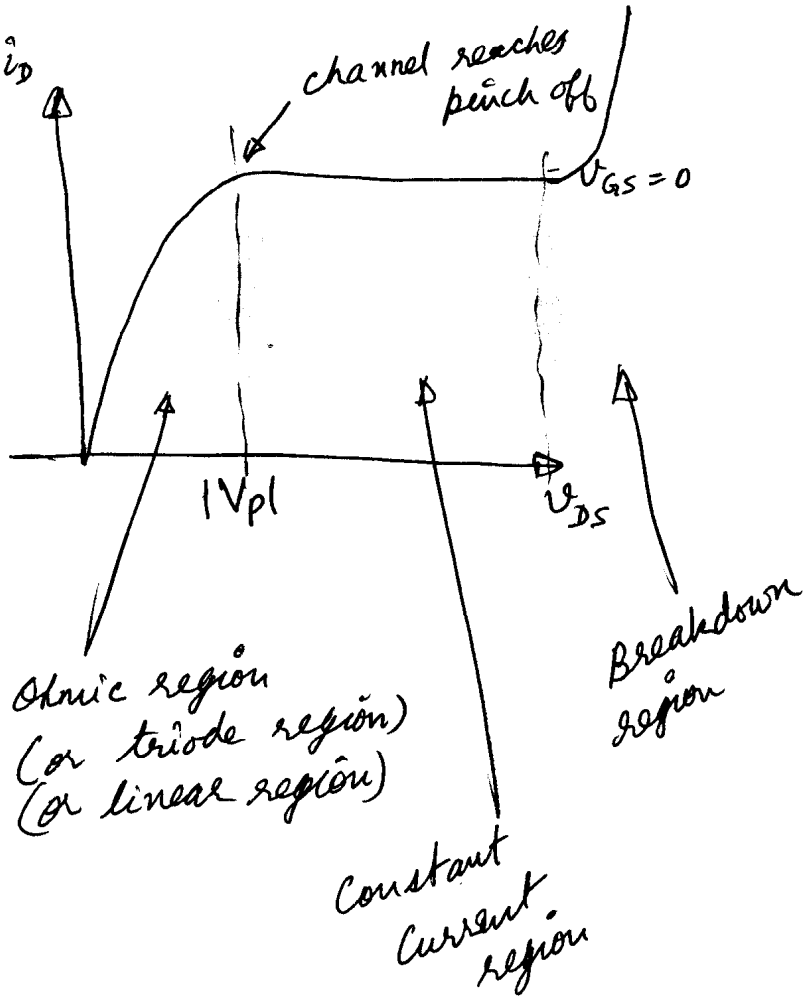
FIGURE 18–28
JFET schematic symbols.

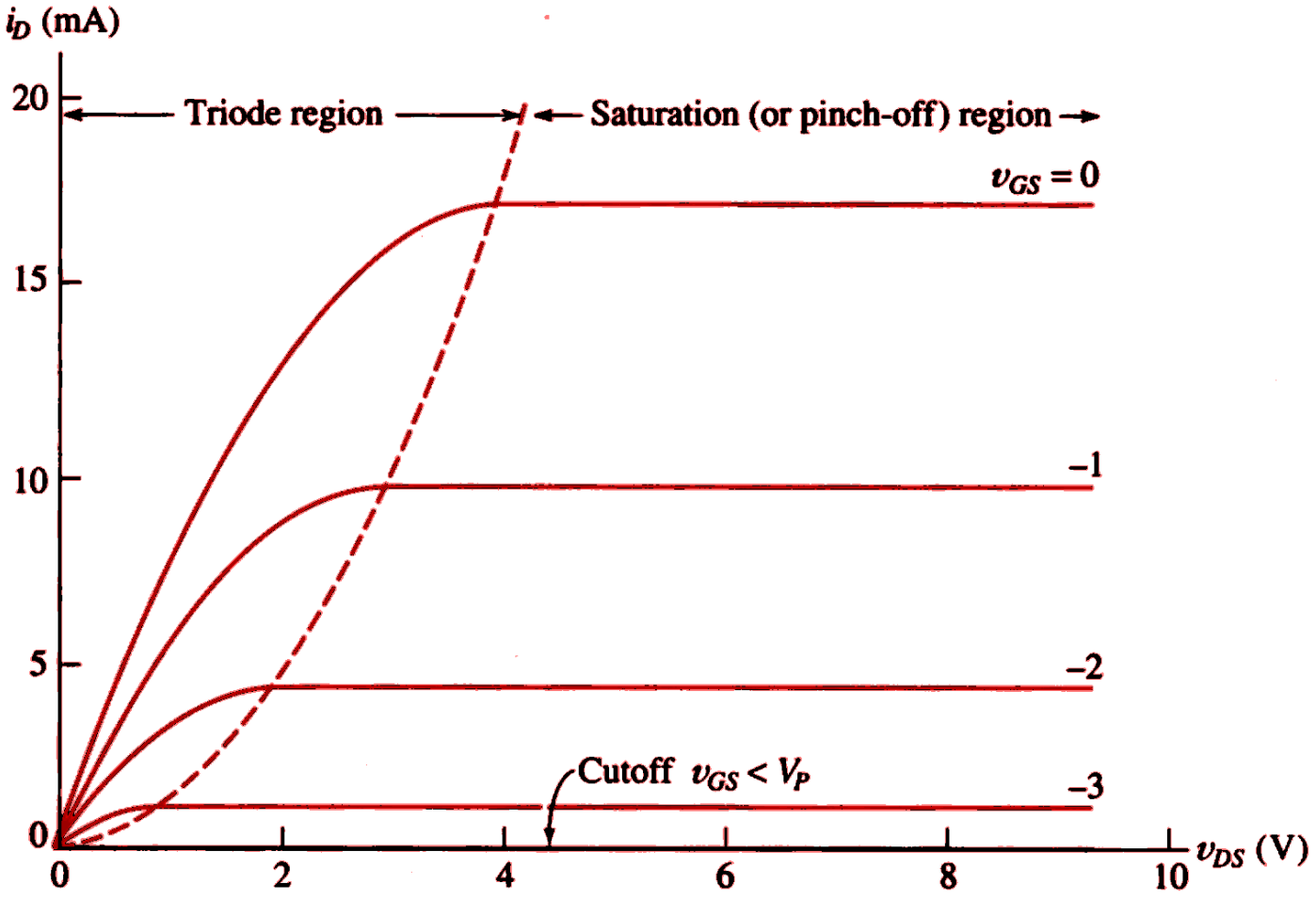


(a) N-channel (b) P-channel

n-channel JFET characteristics







Typical drain characteristics of an *n*-channel JFET.

- **Cut off Region**

(NOTE: V_p is a negative value. e.g in figure 6.6, $V_p = -4V$)

$$v_{GS} < V_p$$

$$i_D = 0$$

- **Linear Region**

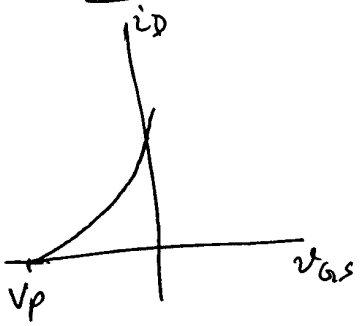
$$v_{GS} > V_p \quad \text{and} \quad v_{GD} = v_{GS} - v_{DS} > V_p$$

$$i_D = k[2(v_{GS} - V_p)v_{DS} - v_{DS}^2]$$

- **Saturation Region**

$$v_{GS} > V_p \quad \text{and} \quad v_{GD} = v_{GS} - v_{DS} < V_p$$

$$i_D = k(v_{GS} - V_p)^2$$



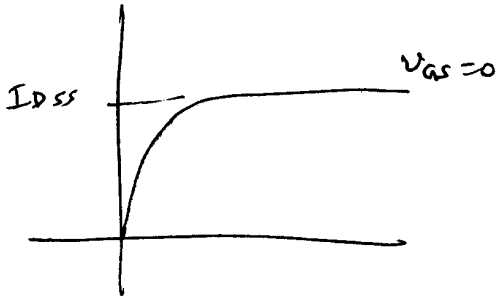
- **Boundary between linear and saturation region**

$$v_{GS} - v_{DS} = V_p$$

$$i_D = k v_{DS}^2$$

- **Zero-bias saturation current I_{DSS} ($v_{GS} = 0$)**

$$I_{DSS} = k V_p^2$$

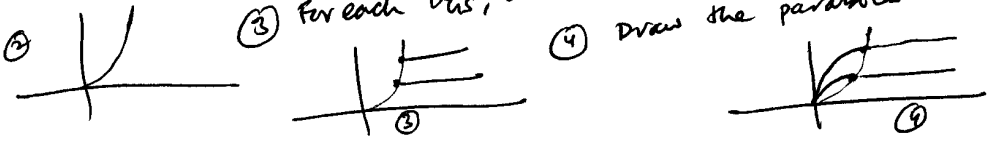


$\therefore$ given I_{DSS} and V_p,

$$k = \frac{I_{DSS}}{V_p^2}$$

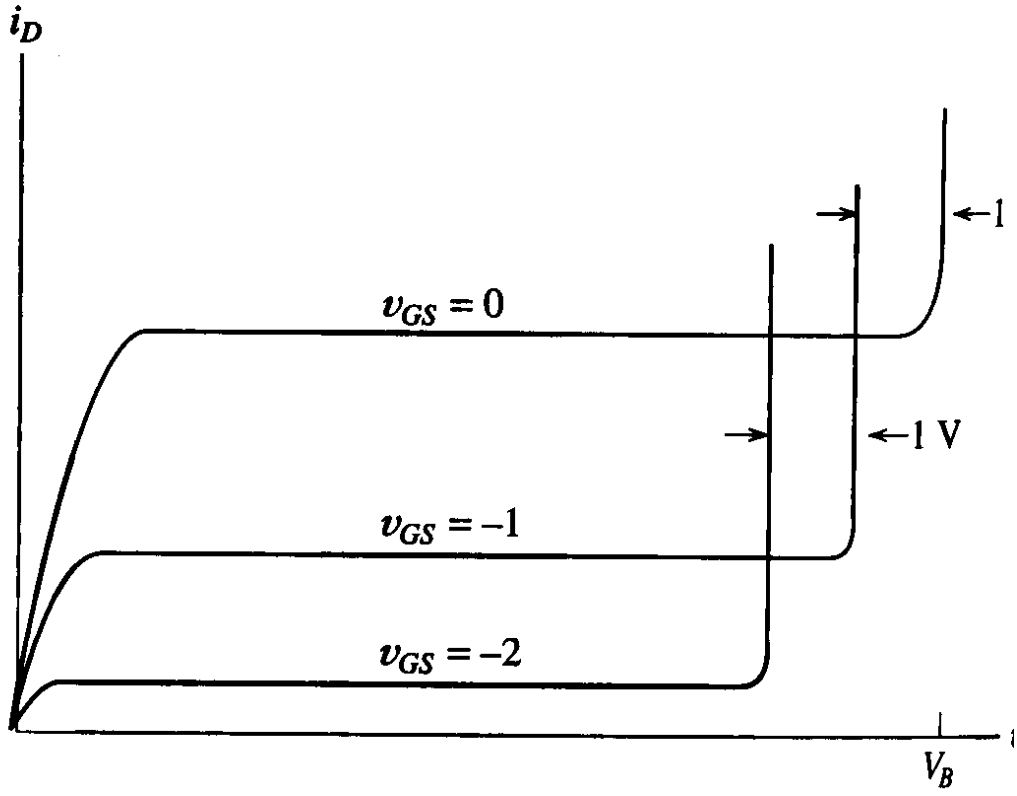
and hence static characteristics of JFET can be plotted.

Example: given I_{DSS} and V_p, ① Calculate k, ② plot Boundary $i_D = k v_{DS}^2$ ③ For each v_{GS}, draw saturation currents, using $i_D = k(v_{GS} - V_p)^2$ ④ Draw the parabolas



BREAKDOWN

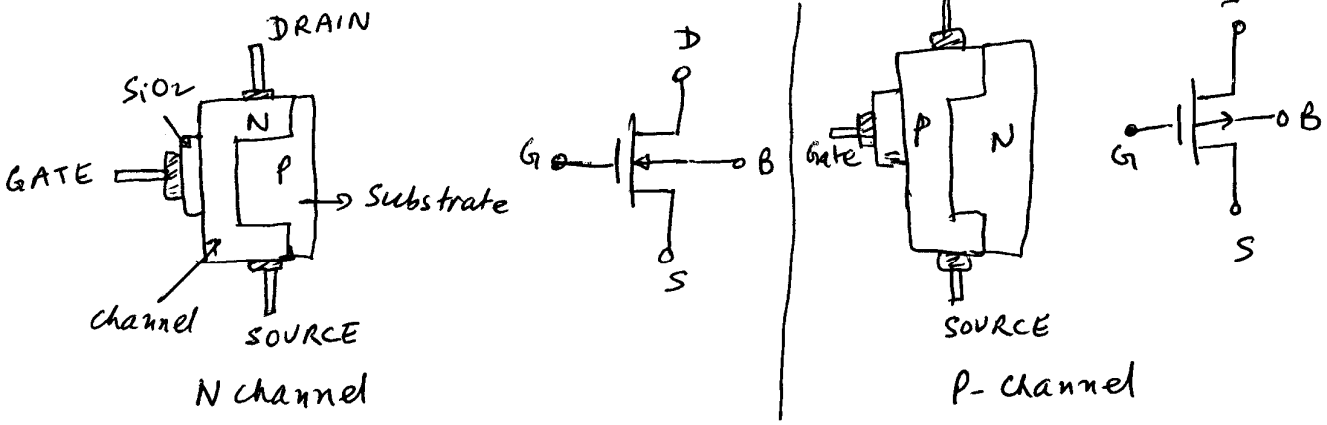
As we mentioned earlier, there are several effects not modeled by tions we have given. An example of one of these effects occurs if th tween gate and channel becomes too large—then the junction experien down and the drain current increases very rapidly. Usually, the greatest the drain end of the channel, so breakdown occurs when v_{DG} exceed voltage V_B in magnitude. Because $v_{DG} = v_{DS} - v_{GS}$, breakdown occurs of v_{DS} as v_{GS} takes values closer to pinch-off. This is illustrated in Fi dom operate FETs in breakdown.

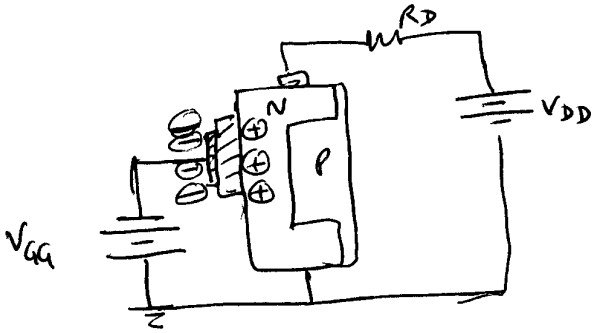


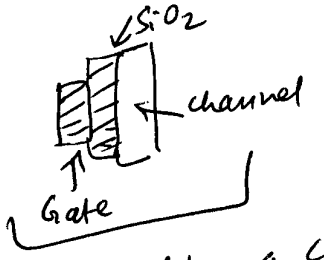
If v_{DG} exceeds the breakdown voltage V_B, drain current increas

MOSFET (Metal Oxide Semiconductor Field Effect Transistor) or IGFET (Insulated Gate FET)

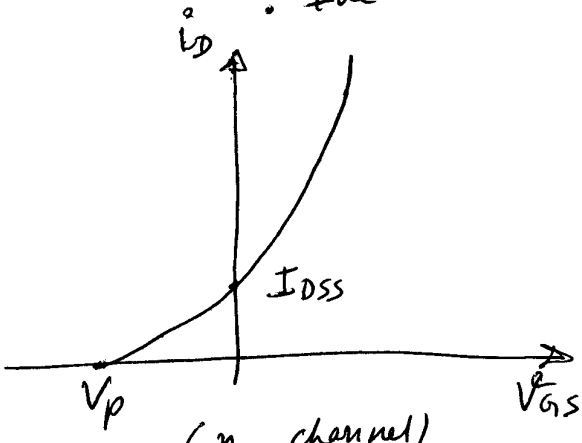
DEPLETION MOSFET (D-MOSFET)



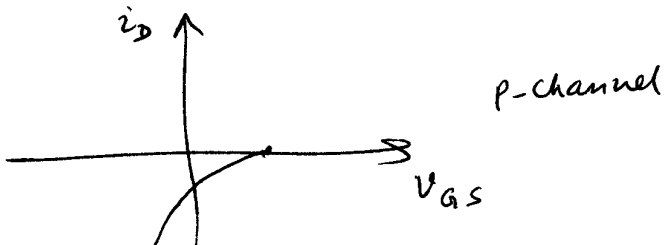




- act like a capacitor
- -ve voltage at Gate induces +ve charge on channel (by attracting holes from P)
- The +ve charge reduces flow
- +ve Gate voltage does reverse.

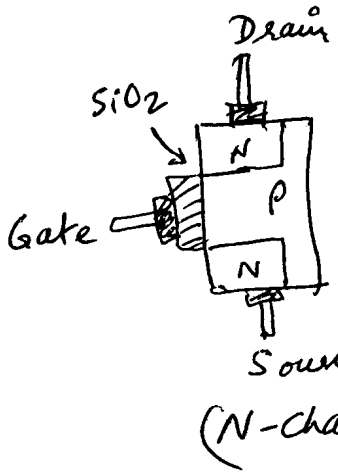


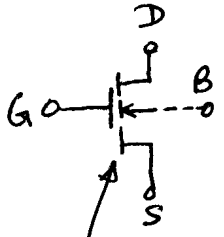
(n-channel)



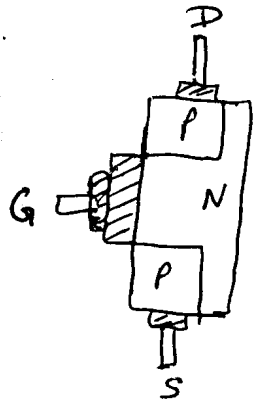
p-channel

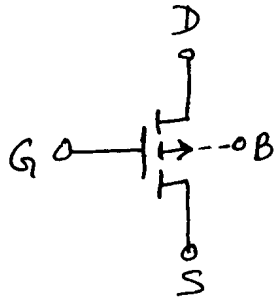
ENHANCEMENT MOSFETs (E-MOSFET)



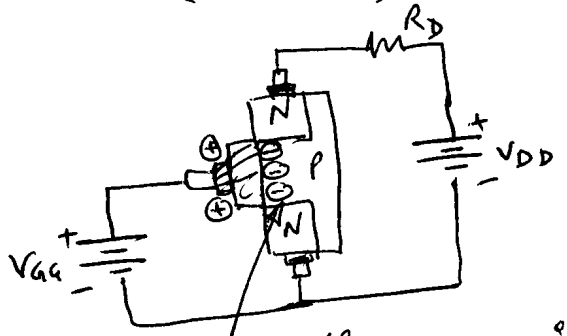


(N-channel) Dashed line

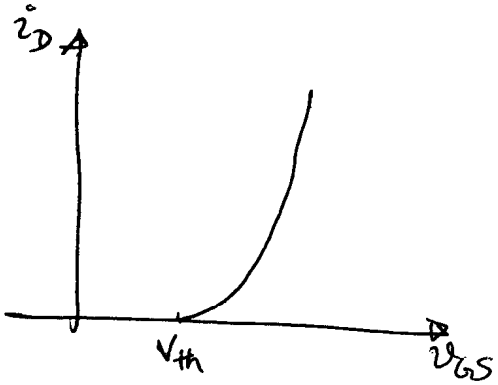




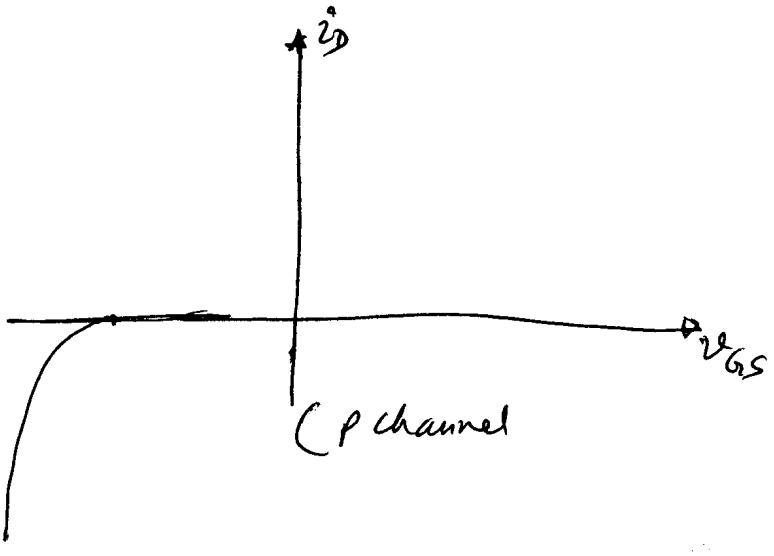
(P-channel)



negative charge increases flow

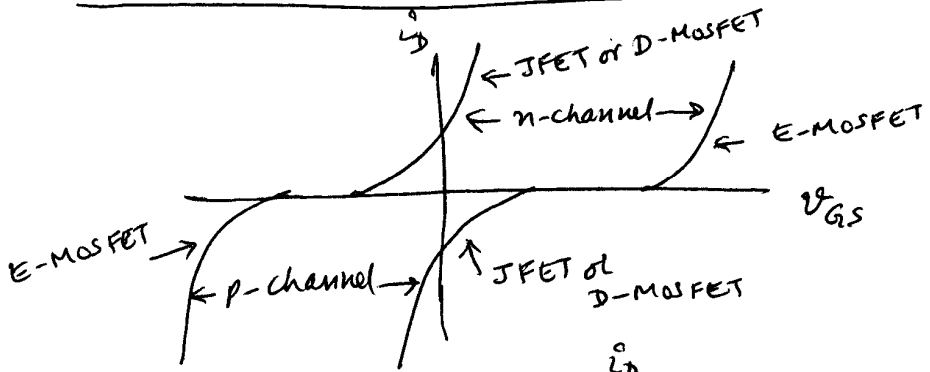


(n-channel)

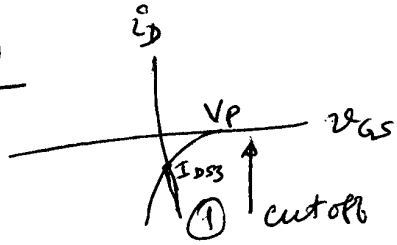


(P channel

Device Equations for p-channel FETs



p-channel (FET)



② Triode Region if

$$\left[\begin{array}{l} v_{GS} < V_P \text{ and} \\ \text{if } v_{GD} = v_{GS} - v_{DS} < V_P \end{array}\right]$$

$$i_D = k\left[2(v_{GS} - V_P)v_{DS} - v_{DS}^2\right]$$

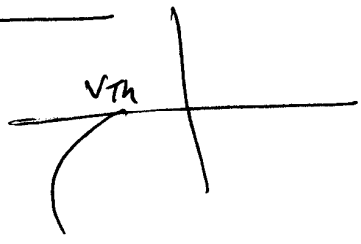
k is negative. $k = \dfrac{I_{DSS}}{V_P^2}$

③ Saturation if

$$\left[v_{GS} < V_P \text{ and } v_{GD} = v_{GS} - v_{DS} > V_P\right]$$

$$i_D = k\left[v_{GS} - V_P\right]^2$$

p-channel E MOSFET

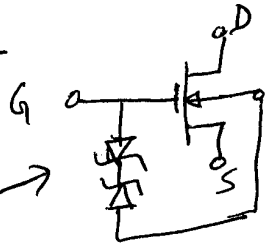


replace V_P by V_{Th}.

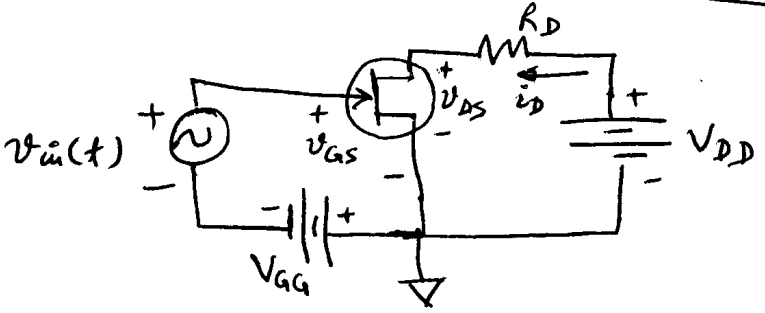
Gate Protection

High input impedance can cause high voltage

To avoid very high damaging voltages →



LOAD LINE ANALYSIS OF JFET CIRCUIT



Example: $V_{DD} = 20V$
$R_D = 1k\Omega$
$V_{GG} = 1V$
$v_{in}(t) = \sin 2000\pi t$

Input loop: $v_{GS} = v_{in}(t) - V_{GG}$ —(1)

$v_{GS} = \sin(2000\pi t) - 1$

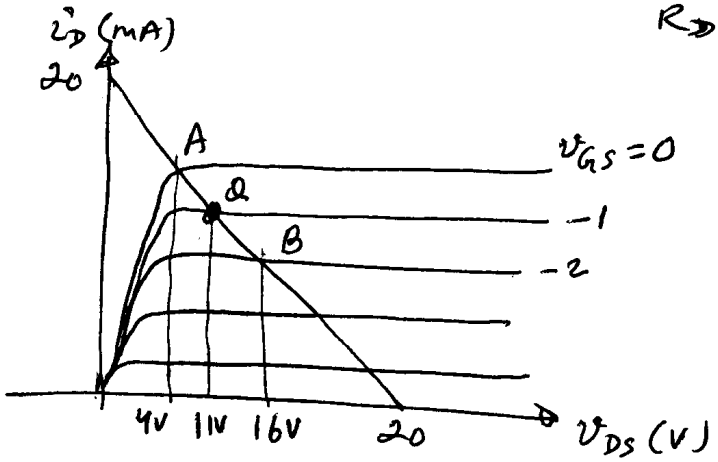
∴ maximum value of $v_{GS} = 0$
minimum " " " $= -2$

Output loop:

$V_{DD} = R_D i_D(t) + v_{DS}(t)$ (Load line equation)

∴ when $i_D = 0 \Rightarrow v_{DS} = V_{DD} = 20V$

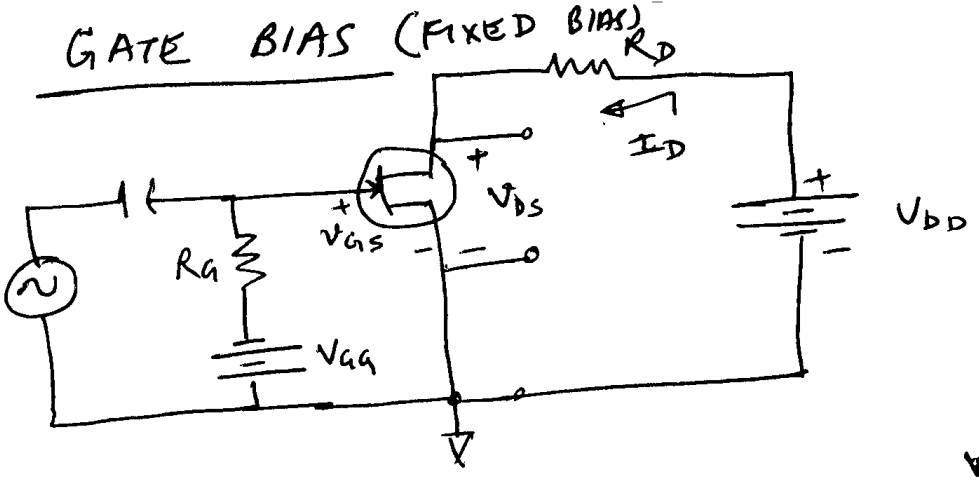
" $v_{DS} = 0 \Rightarrow i_D = \frac{V_{DD}}{R_D} = \frac{20V}{1k\Omega} = 20mA$



Voltage gain $= \frac{4-16}{2-0} = -6$

- FET curves not uniformly spaced (compared to BJT), ∴ more distortion
- More current gain but less voltage gain than BJT
- Very high input impedance

GATE BIAS (FIXED BIAS)



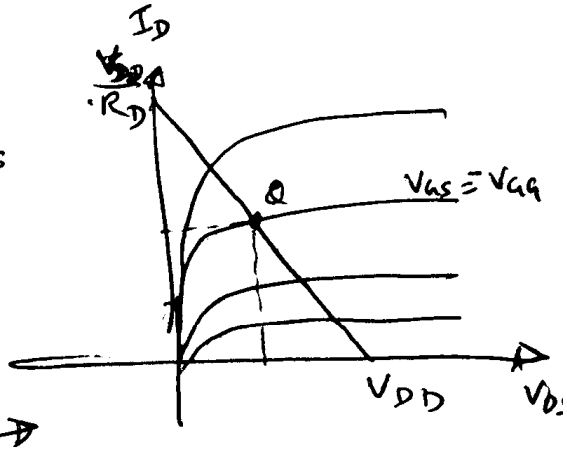
$V_{GS} = -V_{GG}$

load line equation: $V_{DD} = I_D R_D + V_{DS}$

when $V_{DS} = 0 \Rightarrow I_D = \frac{V_{DD}}{R_D}$

$I_D = 0$, then $V_{DS} = V_{DD}$

Load line analysis →



Alternate method:

If I_{DSS} and V_P are given, then

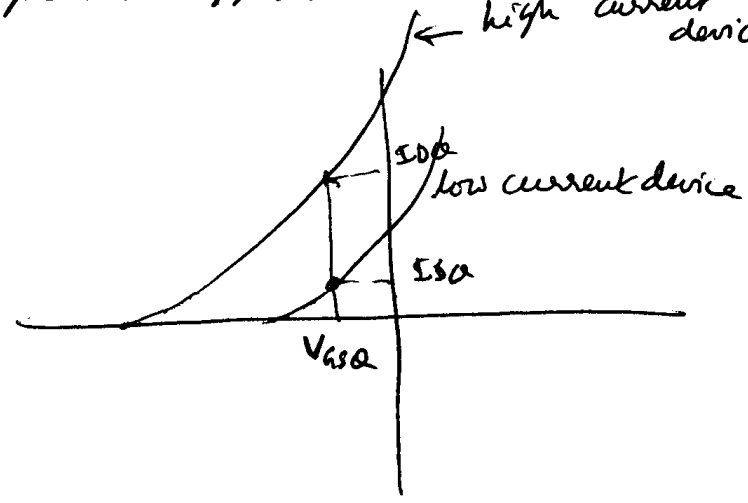
$I_D = K(V_{GS} - V_P)^2$ (assuming pinchoff (saturation) region)

then $V_{DS} = V_{DD} - I_D R_D$

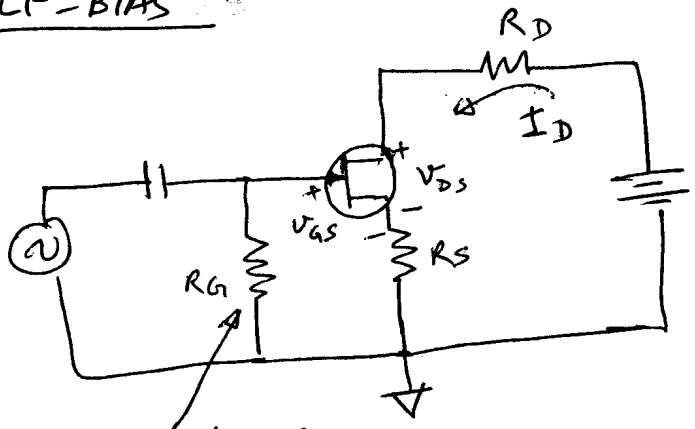
NOT A GOOD BIAS TECHNIQUE, because

- of JFET parameter variations
- of need of two power supplies

I_{DQ} changes for fixed V_{GSQ} for different devices.

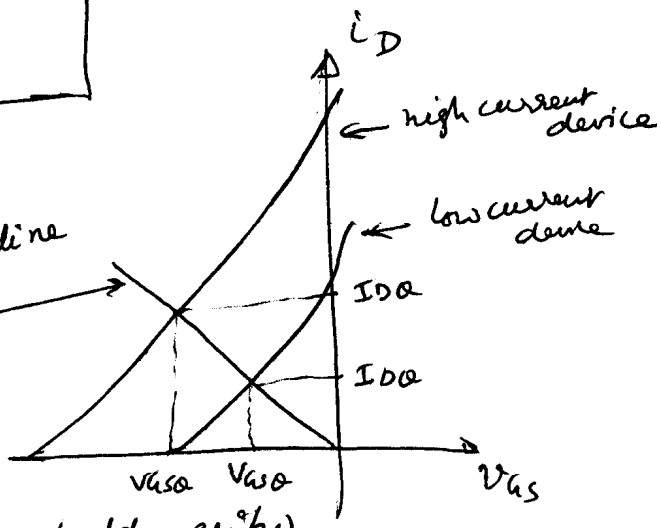


SELF-BIAS



kept for AC (large value)

$$V_{GS} = -R_S I_D$$



Assumption that operation in saturation. (You should verify)

$$I_{DQ} = k(V_{GSQ} - V_P)^2 \quad \text{where} \quad k = \frac{I_{DSS}}{V_P^2}$$

Example: (6.3)

Given $I_{DSS} = 4mA$, $V_P = -2V$, $R_D = 2.2k\Omega$, $V_{DD} = 20V$

$I_{DQ} \cong 2mA$ (use 10% tolerance resistors)

$$k = \frac{I_{DSS}}{V_P^2} = 1mA/V^2$$

$$I_{DQ} = k(V_{GSQ} - V_P)^2$$

$$\therefore (V_{GSQ} - V_P)^2 = \frac{I_{DQ}}{k} = 2$$

$$\therefore V_{GSQ} = -2 \pm \sqrt{2}$$

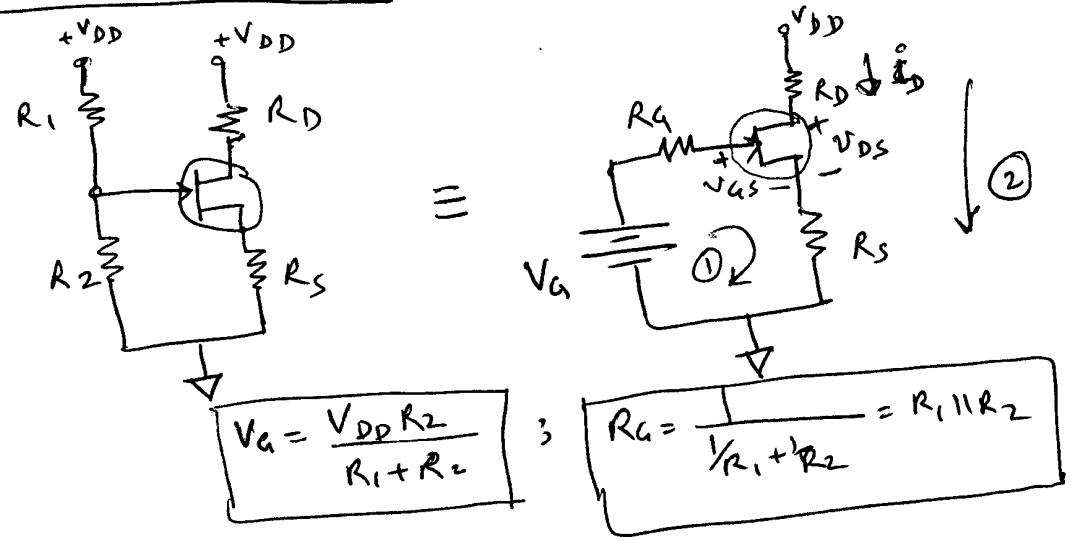
Use $-2 + \sqrt{2} = V_{GSQ} = -0.586V$ ($> V_P$, $\therefore$ in saturation)

$$V_{GSQ} = -R_S I_{DQ}$$

$$\therefore R_S = -\frac{V_{GSQ}}{I_{DQ}} \Rightarrow \text{closest } R_S \text{ to } 293\Omega$$

$$R_S = 270\Omega$$

Voltage-Divider Bias (Fixed-plus-self bias)



$$V_G = \frac{V_{DD} R_2}{R_1 + R_2} \quad ; \quad R_G = \frac{}{1/R_1 + 1/R_2} = R_1 \| R_2$$

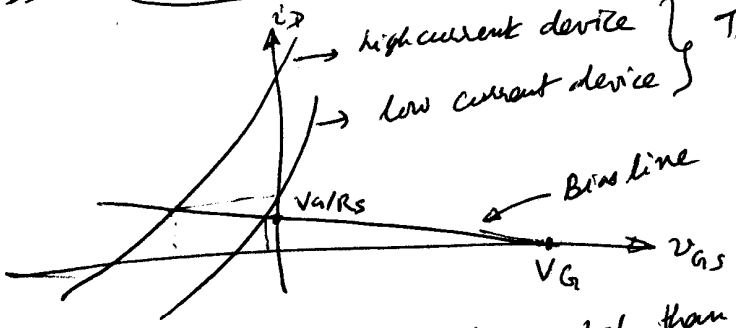
using loop (1)

$$V_G = V_{GS} + i_D R_S$$ ← Bias line equation

$$i_D = k(v_{GS} - V_P)^2$$ ← Transconductance Curve Equation

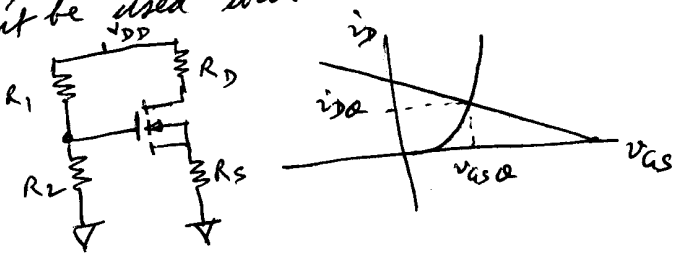
using loop (2) for finding V_{DS}

$$v_{DS} = V_{DD} - (R_D + R_S) i_D$$

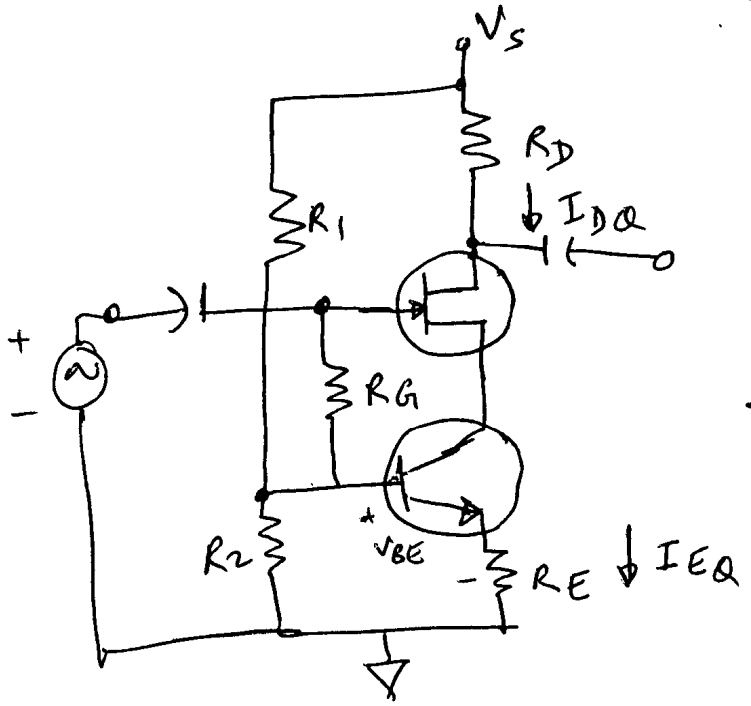


notice bias line more horizontal than self bias.
(larger the V_G value, more horizontal the curve, but V_G can not be too high because that raises voltage drop across R_S, and sufficient voltage must be allocated for v_{DS} and R_D. linear region if v_{DS} is small)

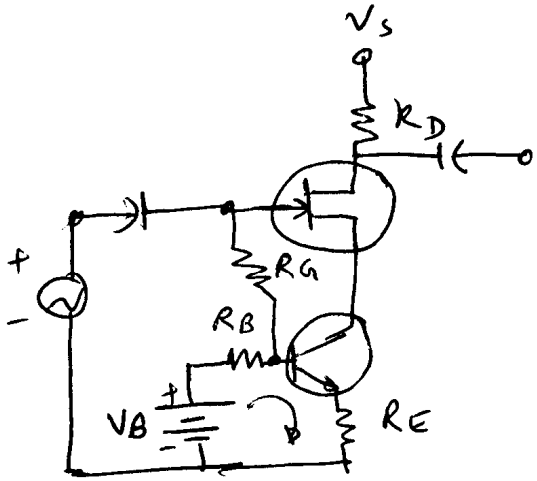
E-MOSFET Biasing: Voltage-divider bias works for E-MOSFETs also because it can create positive V_{GSQ}. (Gate bias and self bias can't be used with E-MOSFETs)



JFET CURRENT SOURCE BIAS



$\equiv$

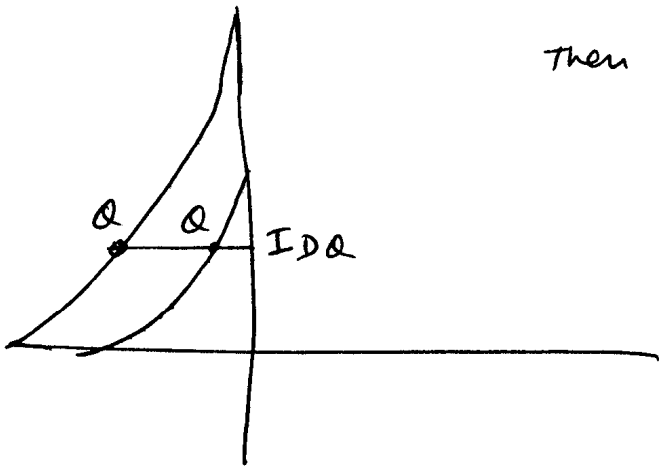


$V_B = I_{BQ}R_B + 0.7 + I_{EQ}R_E$ — ①

$I_{BQ} = I_{EQ}/(1+\beta)$ — ②

obtain I_{EQ} from ① and ②

Then $I_{DQ} = I_{EQ}$

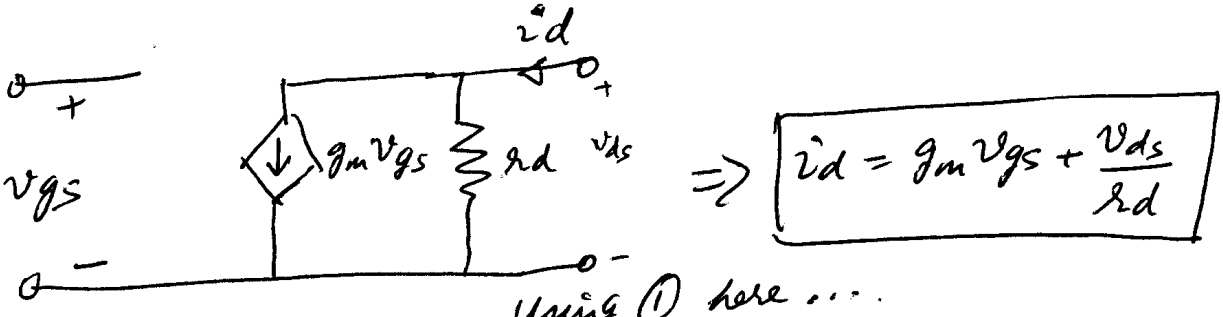


SMALL SIGNAL MODEL FOR FETs

$i_D(t) = I_{DQ} + i_d(t)$; $v_{GS}(t) = V_{GSQ} + v_{gs}(t)$

($i_D(t)$: total signal; I_{DQ}: DC large signal; $i_d(t)$: $\Delta i_D (= i_D(t) - I_{DQ})$)

in saturation: $i_D = K(v_{GS} - V_P)^2$ — (1)



$\Rightarrow \boxed{i_d = g_m v_{gs} + \frac{v_{ds}}{r_d}}$

using (1) here ....

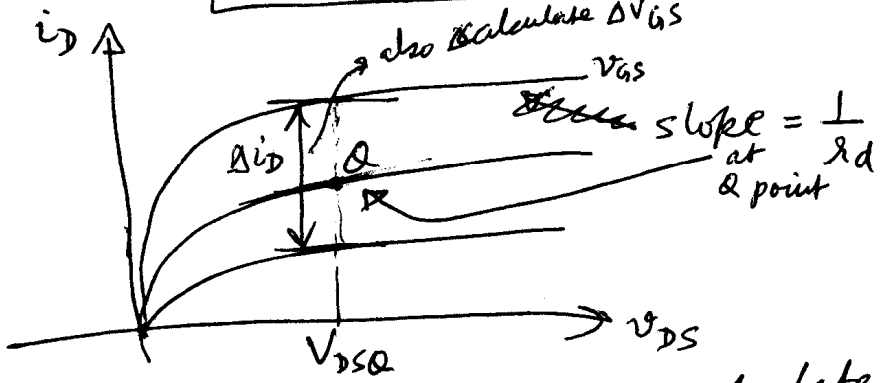
$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{Q\text{ point}} = 2K(V_{GSQ} - V_P) \quad — (2)$$

using (1) at Q point gives

$$I_{DQ} = K(V_{GSQ} - V_P)^2 \Rightarrow V_{GSQ} - V_P = \sqrt{\frac{I_{DQ}}{K}} \quad — (3)$$

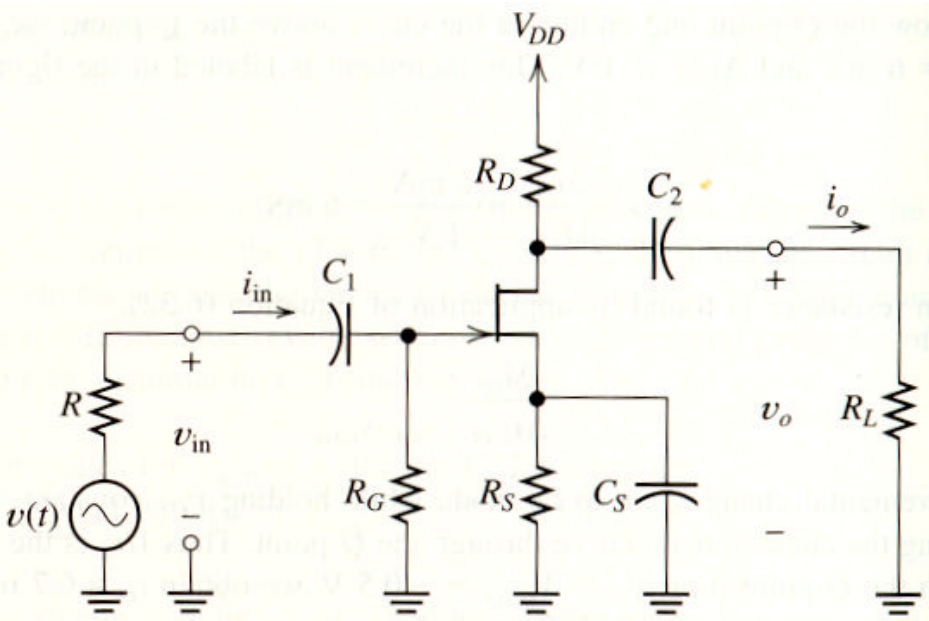
using (3) in (2) gives

$$\boxed{g_m = 2K(V_{GSQ} - V_P) = 2\sqrt{K I_{DQ}}}$$

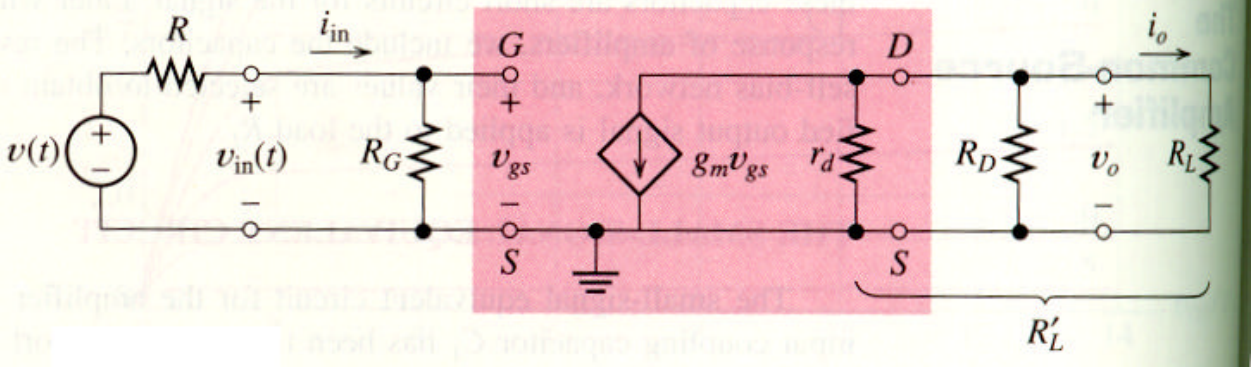


From plot, we can calculate g_m and r_d.

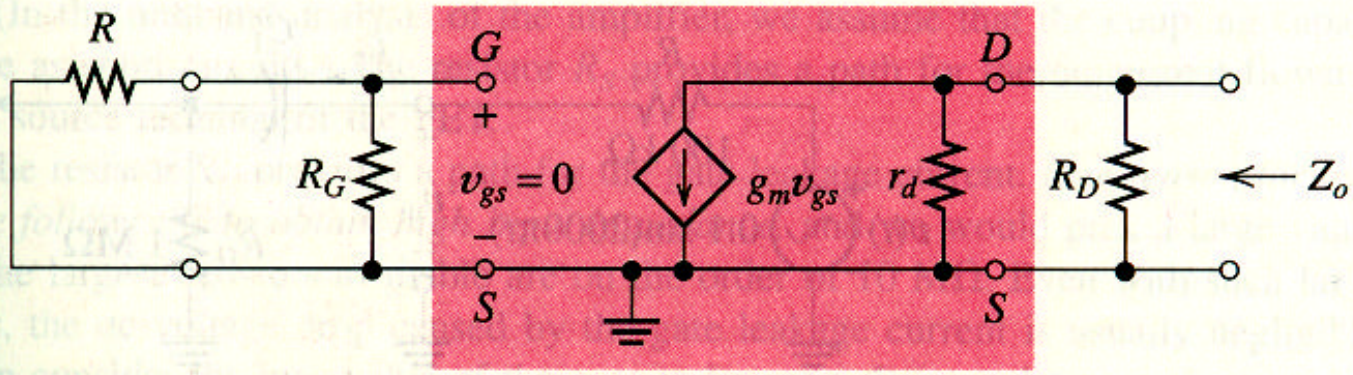
(Sometimes simple model ignores r_d)



Common-source amplifier.



Small-signal equivalent circuit for the common-source amplifier.



Circuit used to find Z_o.

Common Source JFET Amplifier

INPUT RESISTANCE

$$R_{in} = \frac{v_{in}}{i_{in}} = R_G$$

OUTPUT RESISTANCE

From figure,

$$R_o = \frac{1}{1/R_D + \frac{1}{r_d}}$$

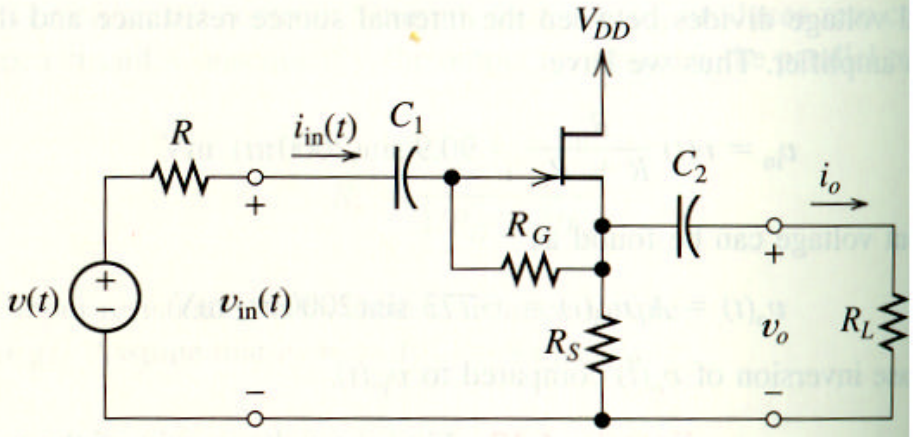
VOLTAGE GAIN

$$R_L' = \frac{1}{\frac{1}{r_d} + \frac{1}{R_D} + \frac{1}{R_L}}$$

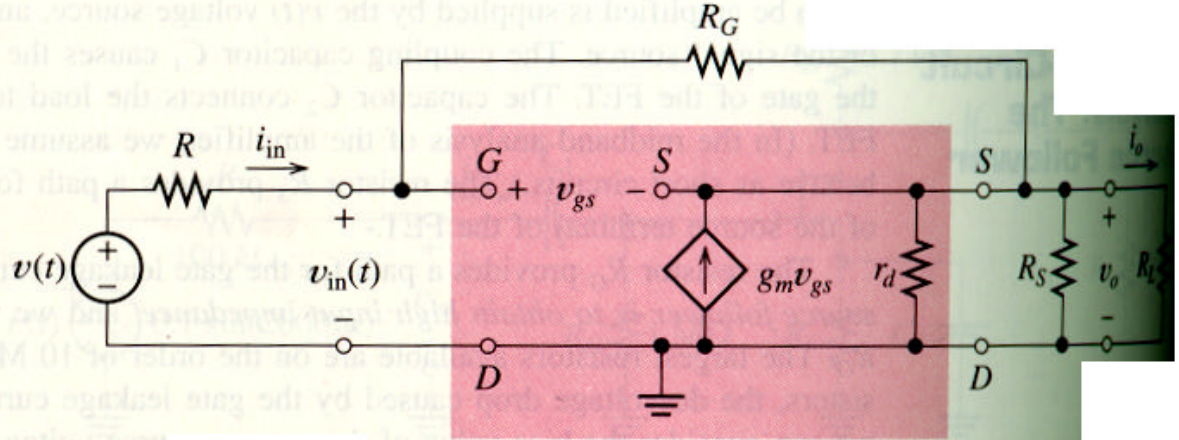
$$v_o = -(g_m v_{gs}) R_L'$$

$$v_{in} = v_{gs}$$

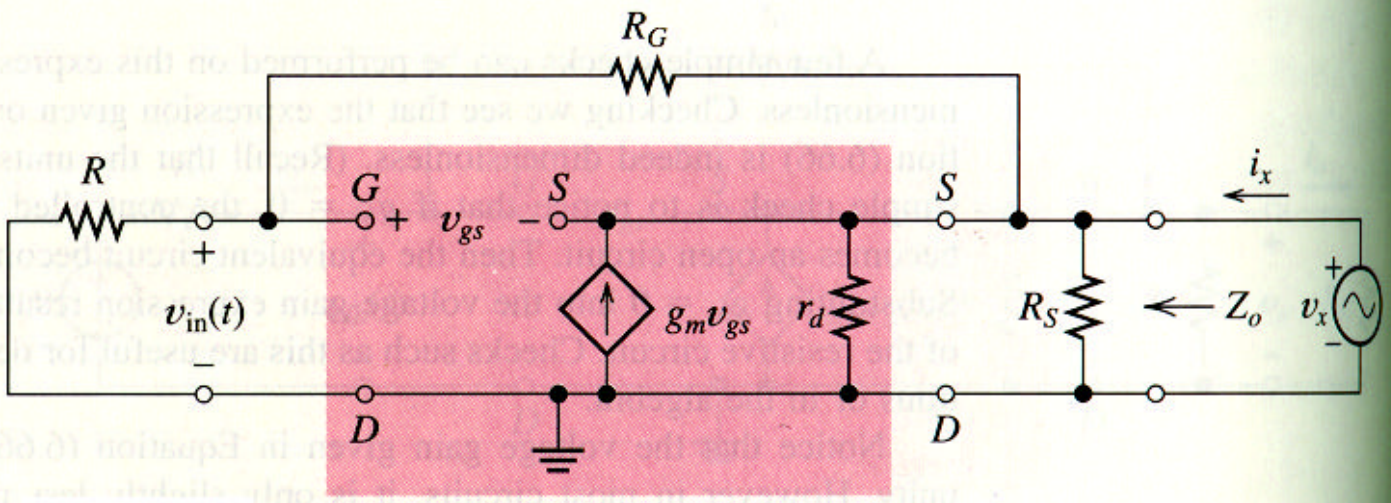
$$\therefore \quad A_v = \frac{v_o}{v_{in}} = -g_m R_L'$$



Source follower.



Small-signal equivalent circuit for the source follower.

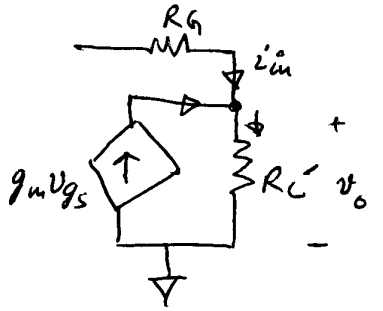


Equivalent circuit used to find the output impedance of the source follower.

Source Follower: (version 1) (High input impedance, low bias stability)

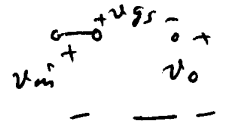
VOLTAGE GAIN:

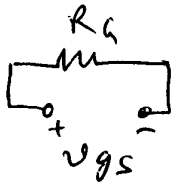
$$R_L' = \frac{1}{\frac{1}{r_d} + \frac{1}{R_s} + \frac{1}{R_L}}$$



$$v_o = R_L'(i_{in} + g_m v_{gs}) \quad -(1)$$

$$v_{in} = v_{gs} + v_o \quad -(2)$$





$$v_{gs} = R_G i_{in} \quad -(3)$$

using (1) and (3)

$$v_o = R_L' i_{in}(1 + g_m R_G) \quad -(4)$$

Using (2), (3) and (4), we have

$$v_{in} = [R_G + R_L'(1 + g_m R_G)]\, i_{in} \quad -(5)$$

Using (4) and (5)

$$A_v = \frac{v_o}{v_{in}} = \frac{R_L'(1 + g_m R_G)}{R_G + R_L'(1 + g_m R_G)}$$

(+ve and slightly < 1 non-inverting voltage follower)

INPUT RESISTANCE

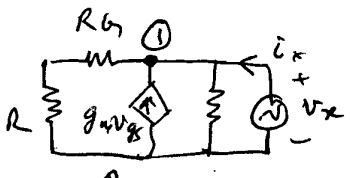
Using (5)

$$\frac{v_{in}}{i_{in}} = R_{in} = R_G + R_L'(1 + g_m R_G)$$

OUTPUT RESISTANCE

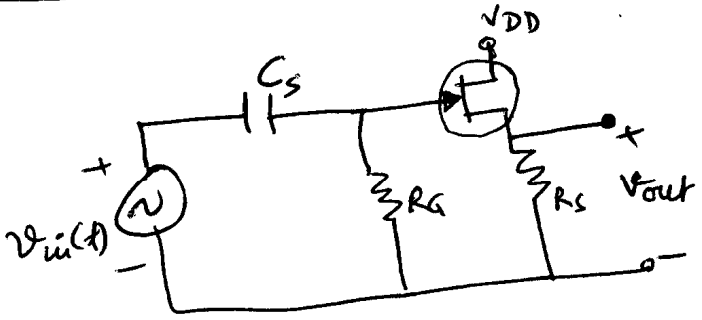
- Remove input source (make it = 0), connect v_x at the output creating i_x, then

$$R_o = \frac{v_x}{i_x} = \frac{1}{\frac{1}{R_L} + \frac{1}{r_d} + \frac{1}{(R_G + R)} + \frac{g_m R_G}{(R + R_G)}}$$

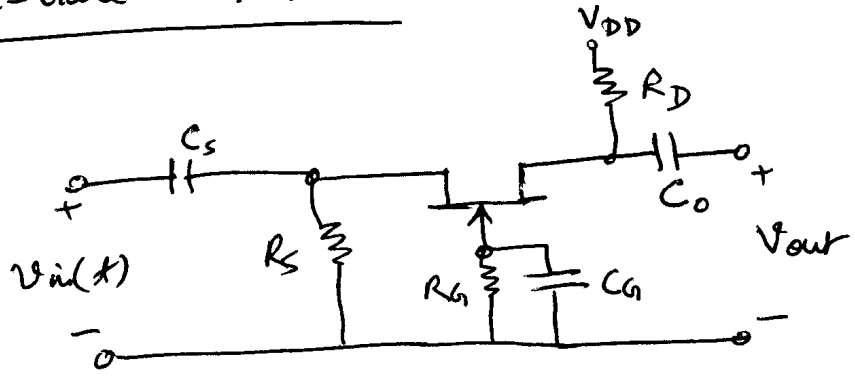


Apply KCL at node ①

Common Drain Amplifier (source Follower - version 2)

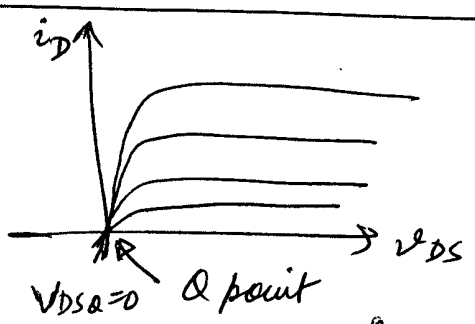


Common-Gate Amplifier



- Used in coupling low impedance source to high impedance load.
- large voltage gain, but current gain close to unity.

FET as a voltage Controlled Resistance



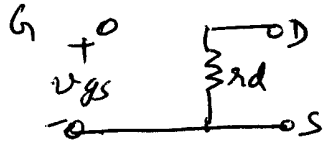
operation in triode region

$$\therefore i_D = K\left[2(v_{GS}-V_P)v_{DS} - v_{DS}^2\right]$$

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{Q\,point} = \left.2Kv_{DS}\right|_{Q\text{-}point} = 0 \quad (\because V_{DSQ}=0)$$

$$\therefore \boxed{g_m = 0}$$

$$\frac{1}{r_d} = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{Q\,point} = \left.K\left[2(v_{GS}-V_P)-2v_{DS}\right]\right|_{Q\,point}$$



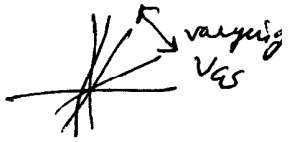
Model for $V_{DSQ}=0$

using $V_{DSQ}=0$, we get

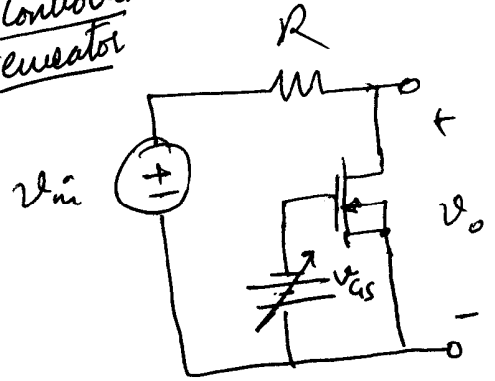
$$\boxed{r_d = \frac{1}{2K(V_{GSQ}-V_P)}}$$

(True if $V_{GSQ} > V_P$ otherwise $r_d = \infty$ (cutoff))

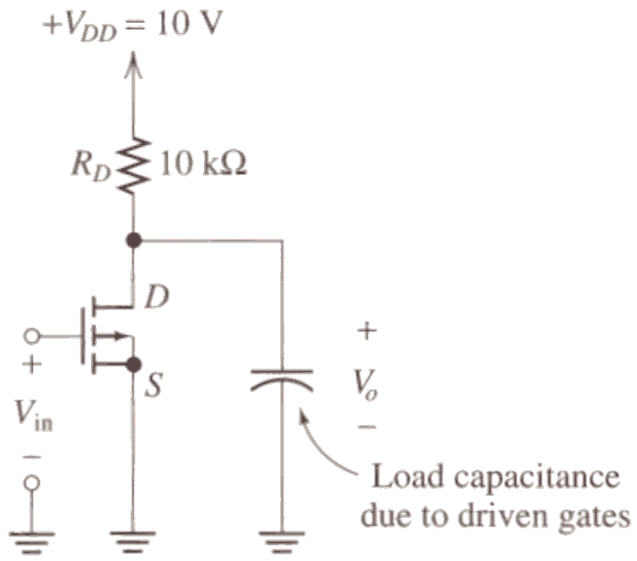
$\therefore r_d$ controlled by V_{GS} (V_{GS} controls slope)



Voltage Controlled Attenuator

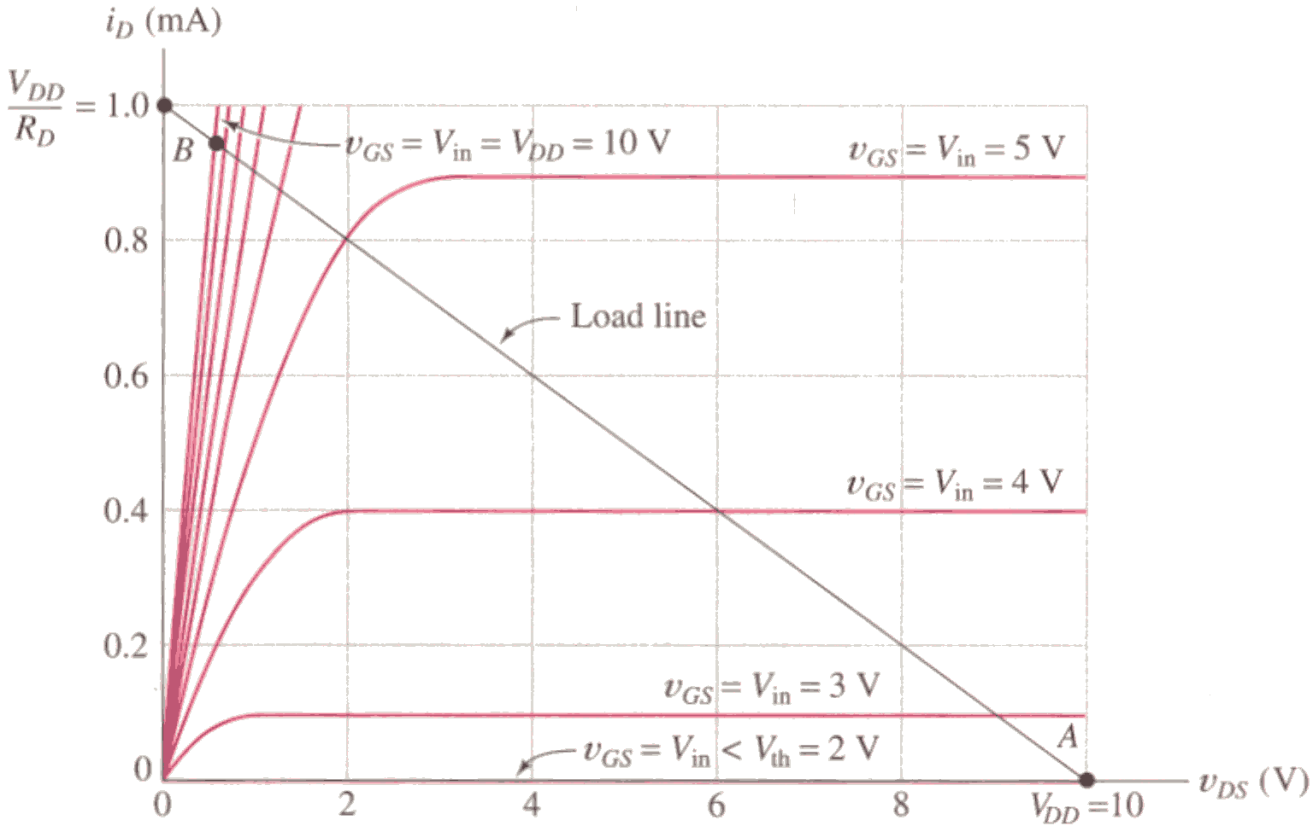


$$\boxed{v_o = \frac{v_{in}\, r_d}{R + r_d}}$$



MOS inverter with pull-up resistor.

In selecting the value of the pull-up resistor R_D, we encounter conflicting objectives. On the one hand, we want to make the resistor large because this leads to a small current when the transistor is on. This, in turn, means a smaller demand on the power supply and less heating of the circuit. On the other hand, we want to make R_D small, so that when the FET switches off, the load capacitance is quickly charged. (Usually, it is important for logic transitions to take place quickly.)



Load-line analysis of MOS inverter with resistive load.

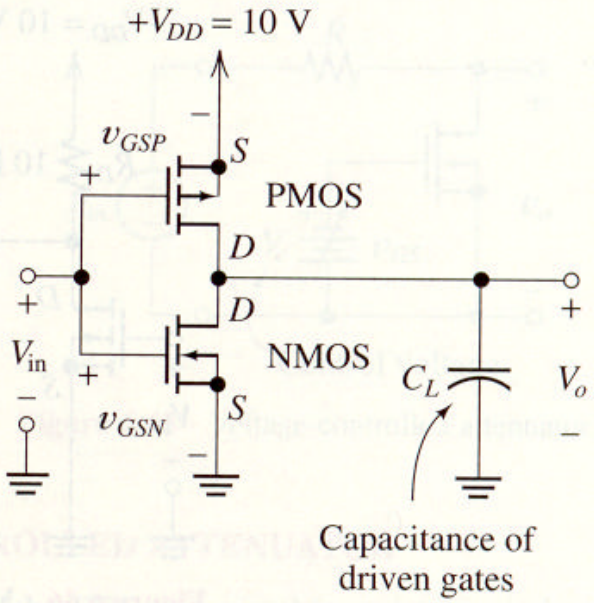


Figure 6.48 CMOS inverter.

THE CMOS INVERTER

A solution to this conflict is to use an enhancement p-channel MOS (PMOS) transistor in place of the pull-up resistor as shown in Figure 6.48. (An additional benefit is that the PMOS takes much less chip area than a resistor and therefore is advantageous for IC implementation.)

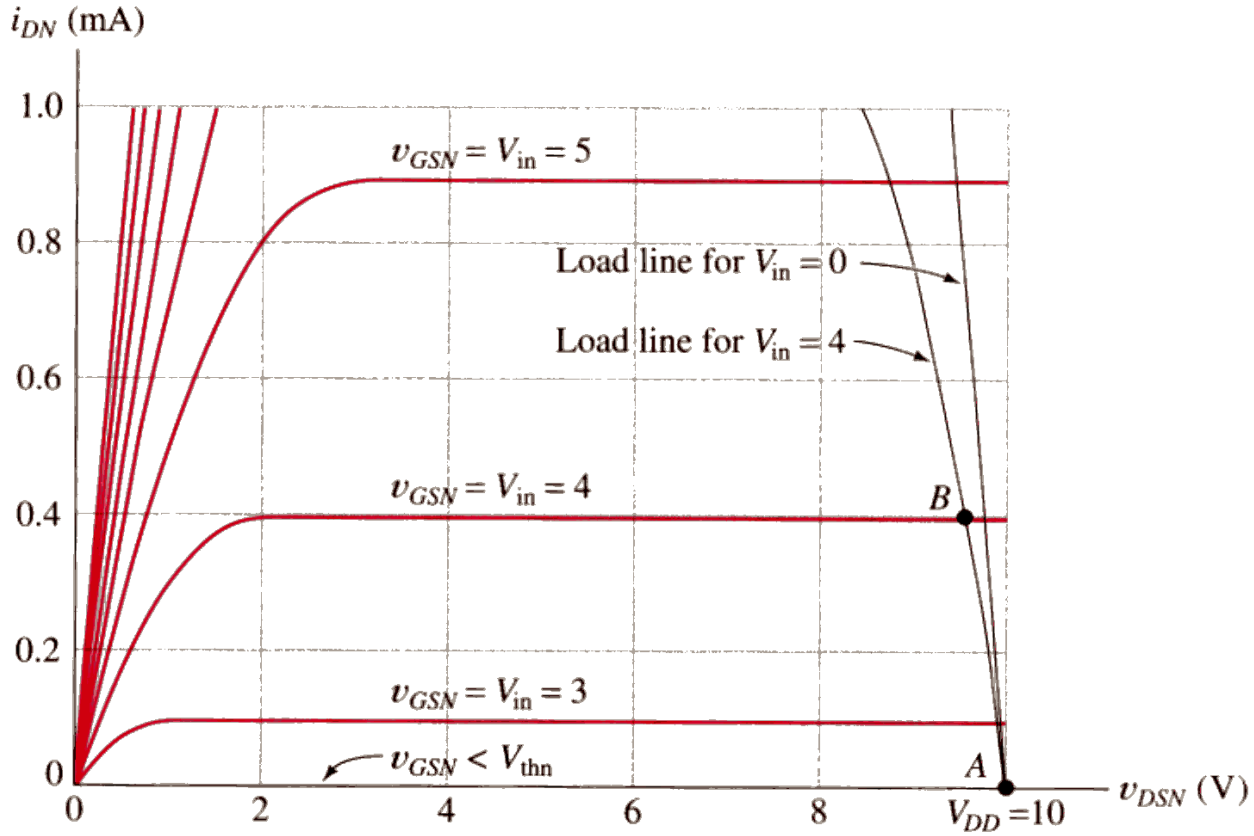
In the following discussion, we assume that except for the differences in voltage polarity and current direction, the NMOS and PMOS have identical characteristics. The threshold of the NMOS is $V_{thn} = V_{th}$, which is a positive value, whereas the threshold voltage of the PMOS is $V_{thp} = -V_{th}$. Also, we assume, as is often the case, that the supply voltage V_{DD} is greater than twice the threshold voltage magnitude. (In the illustrations, we assume that $V_{th} = 2$ V and $V_{DD} = 10$ V.)

Notice in Figure 6.48 that the source terminal of the PMOS is connected to V_{DD}, and the drain is connected to the inverter output. The gate-to-source voltage of the PMOS is given by

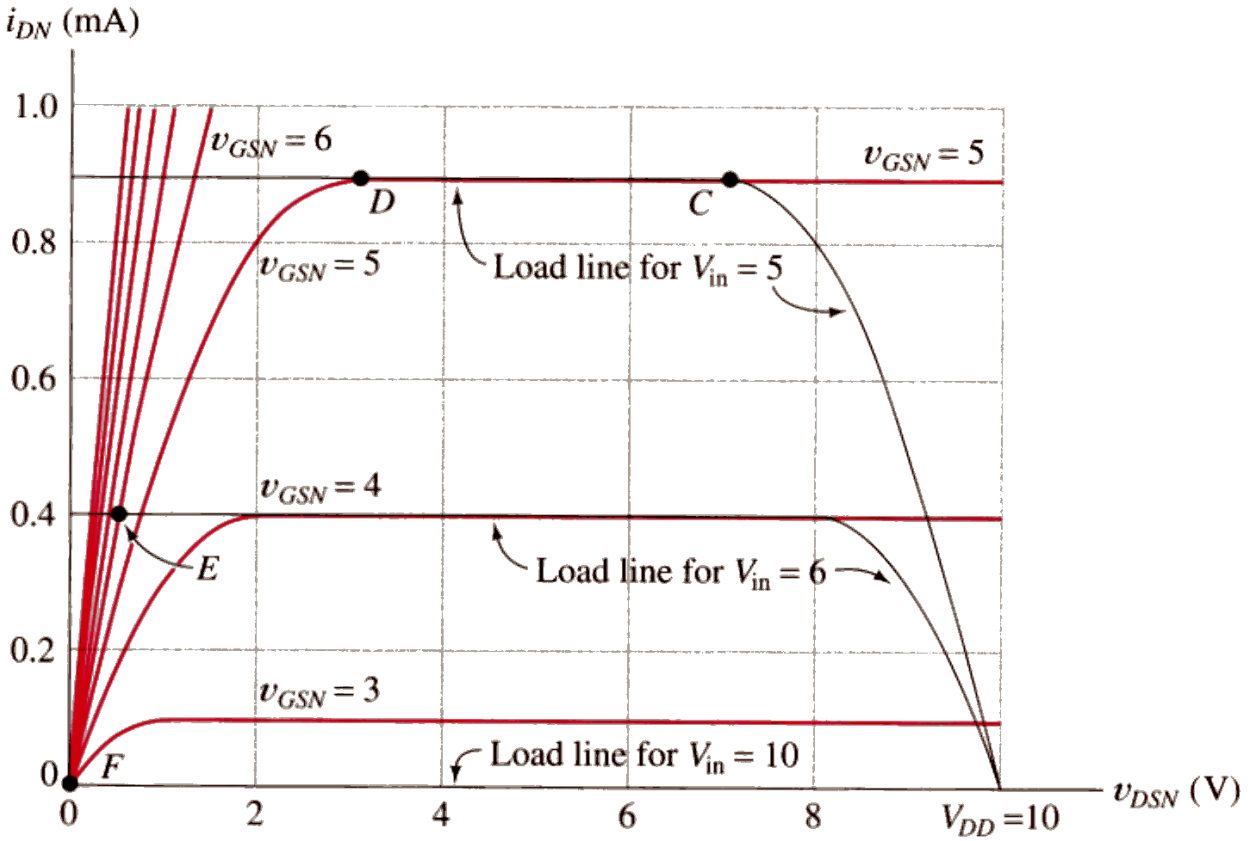
$$v_{GSP} = V_{in} - V_{DD}$$

When $V_{in} = V_{DD}$, the gate-to-source voltage of the PMOS is zero, so it is cut off. Then it acts like a very high value of R_D, and virtually no current flows from the supply. On the other hand, when $V_{in} = 0$, we have $v_{GSP} = -V_{DD}$, and the PMOS can deliver a large drain current to charge the load capacitance. Since the NMOS is cut off for $v_{GSN} = V_{in} = 0$, no current flows after the capacitance is charged.

An important advantage of CMOS logic circuits is that, except during logic transitions, either the NMOS or the PMOS is cut off, and no current flows. Thus the **static power consumption** (i.e., the power consumption of a logic circuit when the logic states are not changing) is virtually zero. For this reason, CMOS is an attractive choice for battery-operated circuits such as portable computers.



(a) $V_{in} = 0$ and $V_{in} = 4$



(b) $V_{in} = 5$, 6, and 10

Figure 6.49 Load-line analysis of CMOS inverter. For the NMOS, $V_{thn} = V_{th} = +2$ V, and for the PMOS, $V_{thp} = -V_{th} = -2$ V.

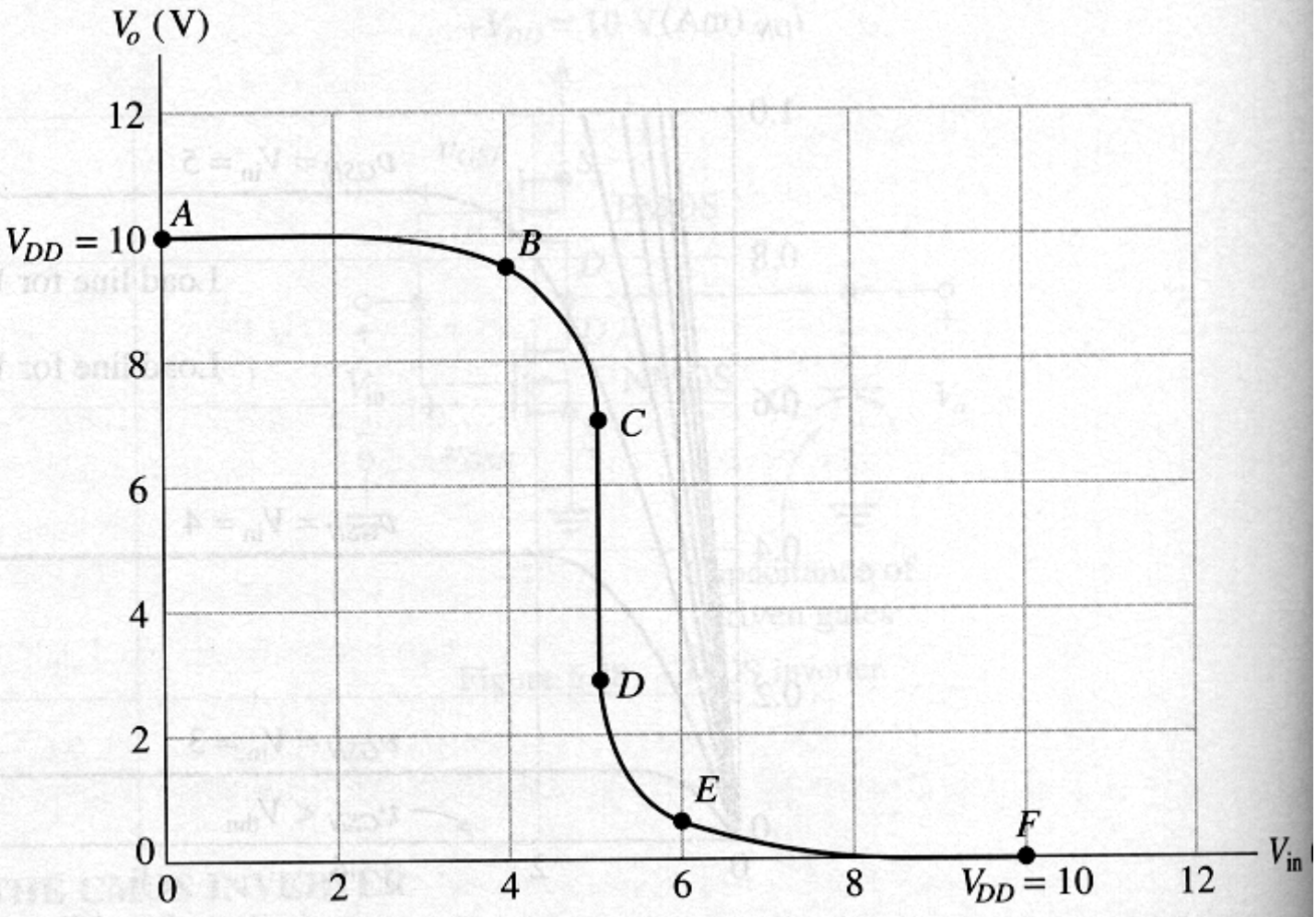


Figure 6.50 Transfer characteristic of a typical CMOS inverter. The lettered points corresp to the points of Figure 6.49.

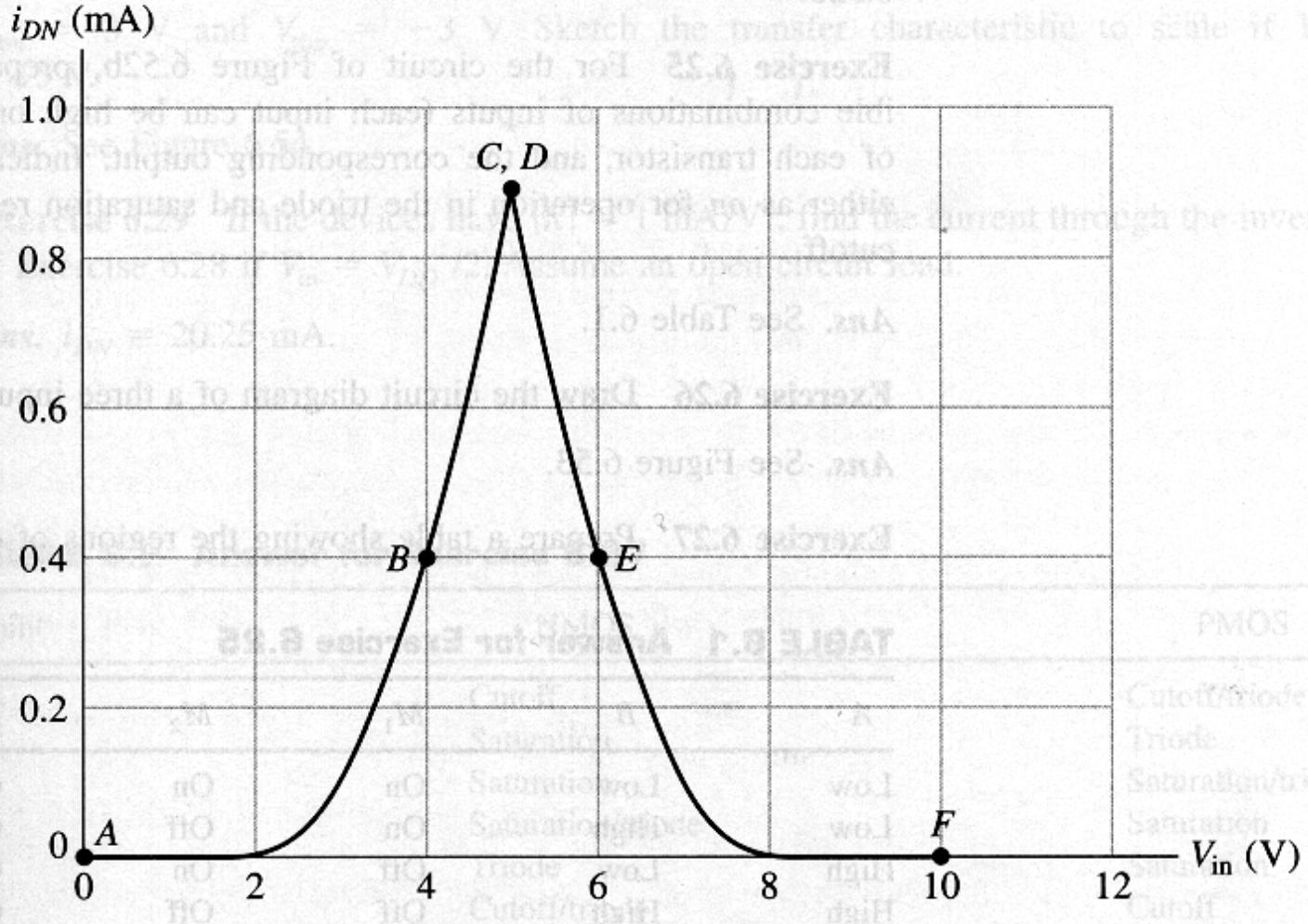
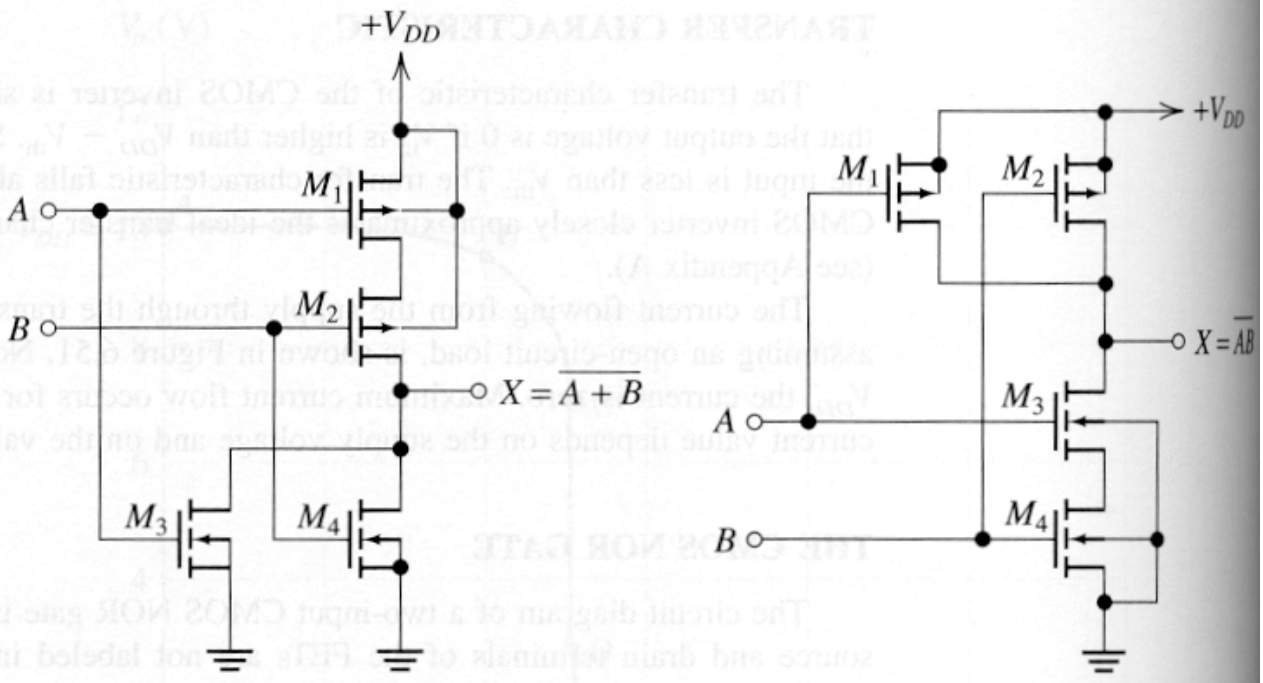


Figure 6.51 Supply current for a CMOS inverter.



(a) Two-input NOR gate (b) Two-input NAND gate

Figure 6.52 CMOS logic gates.

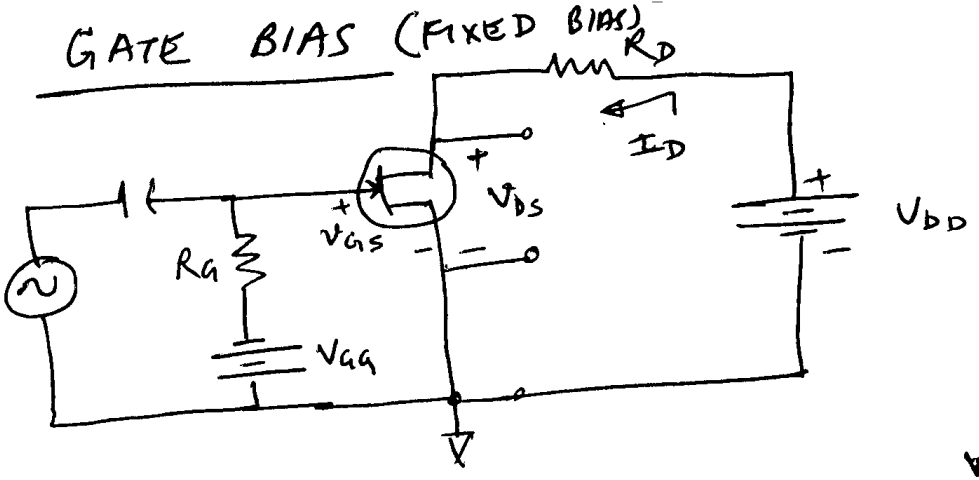
Exercise 6.25 For the circuit of Figure 6.52b, prepare a table showing all possible combinations of inputs (each input can be high or low), the corresponding state of each transistor, and the corresponding output. Indicate the state of each transistor either as *on* for operation in the triode and saturation regions or as *off* for operation in cutoff.

Ans. See Table 6.1.

TABLE 6.1 Answer for Exercise 6.25

A	B	M_1	M_2	M_3	M_4	X
Low	Low	On	On	Off	Off	High
Low	High	On	Off	Off	On	High
High	Low	Off	On	On	Off	High
High	High	Off	Off	On	On	Low

GATE BIAS (FIXED BIAS)



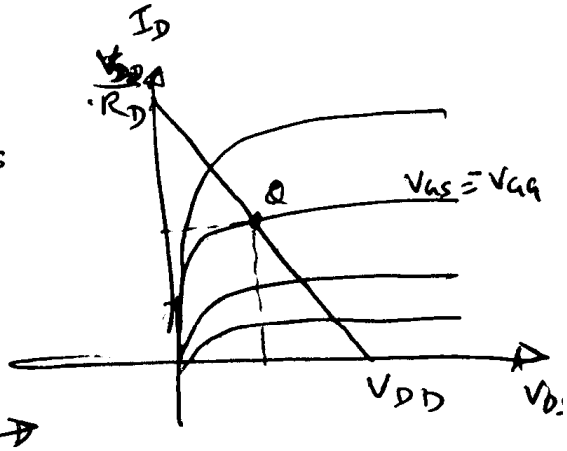
$V_{GS} = -V_{GG}$

load line equation: $V_{DD} = I_D R_D + V_{DS}$

when $V_{DS} = 0 \Rightarrow I_D = \frac{V_{DD}}{R_D}$

$I_D = 0$, then $V_{DS} = V_{DD}$

Load line analysis →



Alternate method:

If I_{DSS} and V_P are given, then

$I_D = K(V_{GS} - V_P)^2$ (assuming pinchoff (saturation) region)

then $V_{DS} = V_{DD} - I_D R_D$

NOT A GOOD BIAS TECHNIQUE, because

- of JFET parameter variations
- of need of two power supplies

I_{DQ} changes for fixed V_{GSQ} for different devices.